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Efficient Layout Design of 4-Bit Full Adder using Transmission Gate

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***Abstract*— In any digital circuit surface area and power both are very important parameters. In this paper 4- bit full adder using transmission gate is designed. To design 4- bit full adder two methods are used. First is semi custom design method and second is full custom design method. In first semi custom design method a layout of 4-bit full adder is designed with available width and length of the transistor. In full custom design method create a layout with the help of reduced width of transistor. 4-bit full adder has one important element which is full adder. Full adder is designed based upon transmission gate. Transmission gate is used to improve the logic level of signal. 90nm technology is used to simulate these two design methods. It can be found from the simulated results that full custom design layout results in 29.65% reduction of surface area of 4-bit full adder as compared to semi custom design. It can also be observed from the simulated results that full custom layout results in 26.22% reduction of power as compared to semi custom design.**

***Keywords*— ADDER, MICROWIND, TRANSMISSION GATE, VLSI**

I. INTRODUCTION

Addition is a basic arithmetic operation that is mainly used in very large scale integration (VLSI) systems its application is in digital signal processing architecture and also in microprocessors. This module is main part of many arithmetic calculations such as multiplication, division addition, and subtraction. Power is one of the most important features for current electronic systems designed for high performance for portable devices. Increasing market demand for the portable electronic devices. So, portable devices should work on low power. The power delay product relates with the energy spent at the time of determined task [1]. Power consumption is an important factor in creation of very large scale integrated circuit with the continuous increase of VLSI technology the demand of portable devices has forced to designer to create smaller silicon area, low power consumption, longer battery life and more reliable electronic circuit [2]. The high speed and reduced surface area of silicon can be designed with different combination of the logic in VLSI. In current time many adder, subtractor circuits proposed that offer low power dissipation, low surface area and low power delay. Increasing demand for battery operated applications; power consumption is a very important factor [3].

Uses of the portable device which based on battery increase daily such as notebook, cellular phone. It demands very large scale integration design with an increased power delay characteristics [4]. The ability of find a design that ensures small latency and low power consumption in modern VLSI design [5].The VLSI implementation of an adder has obtained great attention from researchers since addition is most frequently used operation in digital circuit systems [6]. The circuit delay is obtained by number of transistors in series, transistor sizes. Transistor size determines the power consumption total area of circuit and also speed of circuit. VLSI design is attracting attention of designers because of emerging need for minimization of silicon surface area, power consumption and performance in nanometer scale is the requirement of present time [7].

II. 4- BIT FULL ADDER

Binary addition is one of the common used applications in computer arithmetic. Demand of decimal arithmetic in many applications such as commercial, internet or financial field. The use of simplest and easy becomes very important for arithmetic operation [8]. Full adder is used in addition, subtraction and multiplication kind of operations. These are key elements in the digital circuit. These performances affect the whole system. In computation these address are the key components whose performance affects the whole circuit [9]. The high improvements in the applications of circuits are the driving force to get new ways in the creation of high performance circuit design. Most of the applications in integrated circuit required arithmetic and logic circuits for calculation [10]. 4-bit full adder using transmission gate block diagram shows in fig. 1.

Fig. 1 Block diagram of 4- bit Full Adder using transmission gate.

A_0, A_1, A_2, A_3, B_0, B_1, B_2, B_3 are the input bits and C_{IN}, C_0, C_1, C_2, are the carry bits of inputs, S_0, S_1, S_2, S_3 are the sum bits of output C_3 is the carry bit of output.

The adder is also known as a full adder. It determines a one bit carry and sum from the two addends and one carry input. The full adder has following equations for sum and carry–

$$S_i = a_i \oplus b_i \oplus c_i \quad (1)$$

$$C_{i+1} = a_i b_i + a_i c_i + b_i c_i \quad (2)$$

S_i = Sum output at i^{th} satge.

C_{i+1} = carry output of the i^{th} stage.

The adder of n- bit make with n one bit full adders is called as a n- bit ripple carry adder or n-bit full adder because of the process the carry is calculated [11]. Binary adders are widely used in digital circuit. It acts as main role in finding the performance of the digital design. Hence developing an efficient adder is crucial to improving the efficient design [12]. For signal processing full adder is the basic logic circuits which can work in computing. The increase in the number of transistors in digital circuit has affects the performance of computing system [13].

An N-MOS transistor is a perfect switch when passing 0 and thus we say it passes a strong 0 but it is imperfect in passing 1. So, it degraded logic 1 similarly P-MOS transistor perfect in passing 1 but it degraded in passing 0. When an N-MOS or P-MOS is used along as a pass transistor. If combined a P-MOS and an N-MOS transistor in parallel. When a 1 is applied to gate of N-MOS. In this both 0's and 1's are passed in an acceptable manner. It known as a transmission gate. It is basically used to strength the logic 0 and logic1 [14]. XOR is one very important element in full adder design. XOR is designed with the help of transmission gates. Multiplexers are also designed with transmission gates to select the sum and carry output. The schematic of 4-bit full adder using transmission gates. It shows in fig. 2. It is circuit level design for 4-bit full adder using transmission gate.

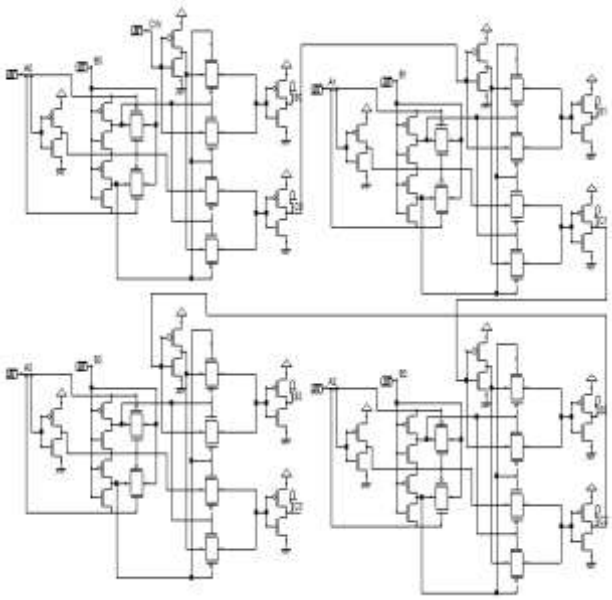

Fig. 2 Circuit level design of 4- bit full adder

The timing diagram of 4-bit full adder using transmission gate shows in fig. 3. It shows the behavious of the circuit.

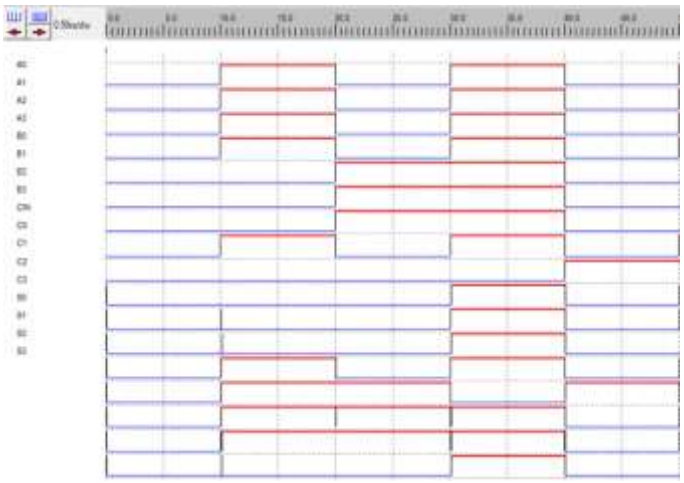

Fig. 3 Timing diagram of Circuit level design

In this paper two design methods are used to design 4-bit full adder using transmission gate. First is Semi custom design method in which we select the transistor as available. Second method is full custom design in which width of the transistor can change which helps in reduction of surface area of the 4-bit full adder using transmission gate. N-well is also helpful in reduction of 4-bit full adder using transmission gate.

III. Semi Custom Design

Semi custom design is the first design method. Layout of 4-bit full adder using transmission gate is designed on Microwind 3.1. The layout design of 4-bit full adder using transmission gate shows in fig. 4. In this design available width of transistor in library is used.

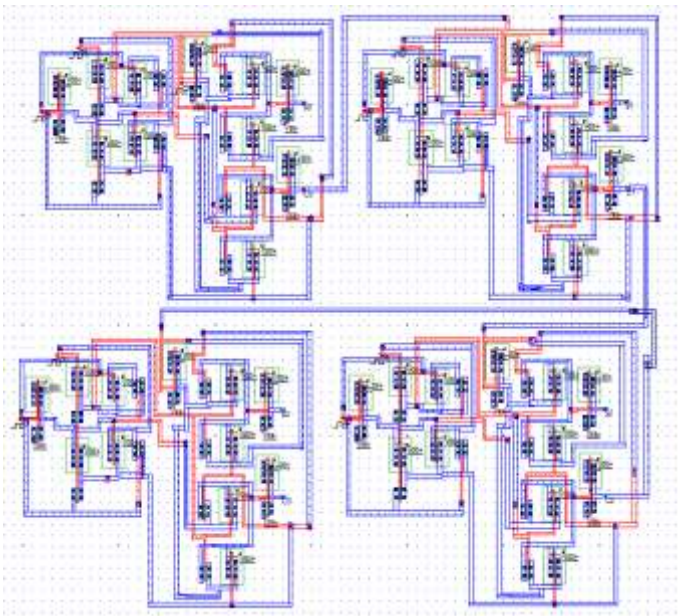

Fig. 4 Layout of Semi custom Design for 4-bit Full Adder

The analog simulation of 4- bit full adder using transmission gate shows in fig. 5. It shows the behaviour of 4-bit full adder with semi custom design method. It also shows the power in milliwatt in the semicustom design. Power consumption in semicustom design method is 0.244 mW.

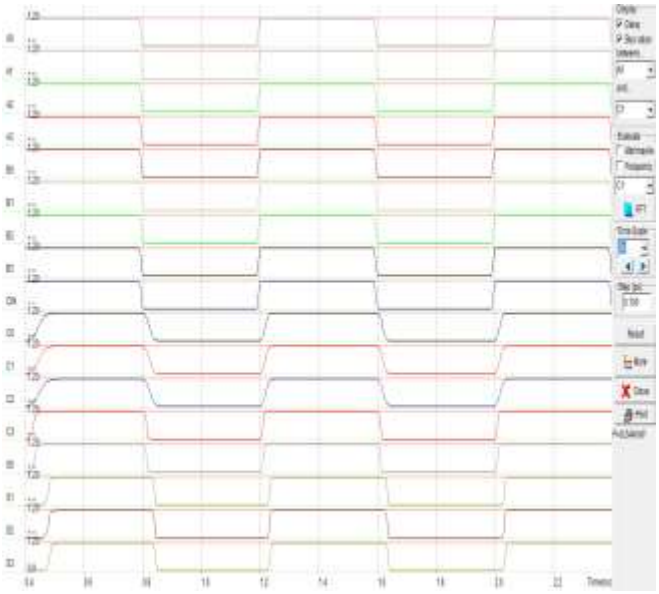

Fig. 5 SPICE Simulation Semi custom design .

IV. Full Custom Design

Full custom design is the second design method. Layout of 4-bit full adder using transmission gate is designed on Microwind 3.1. The layout design of 4-bit full adder using transmission gate shows in fig. 6. In this design method the size of P-MOS and N-MOS in term of its width is less as comparison to the semi custom design. It is helpful in reduction of area of layout. N-well is used to reduce the surface area of the 4-bit full adder using transmission gate.

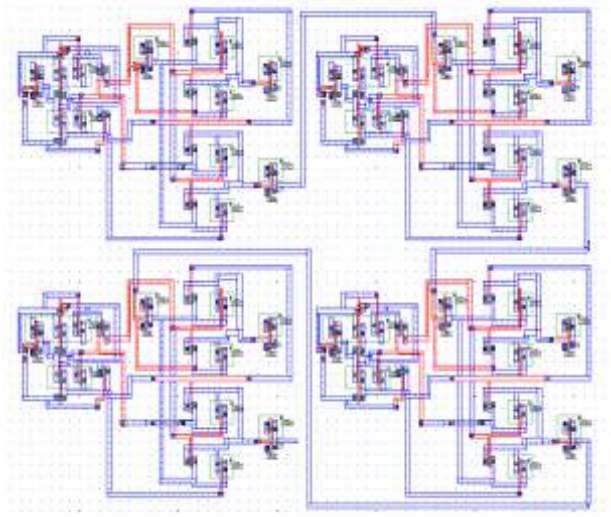

Fig. 6 Layout of Full Custom Design for 4-bit Full Adder

The analog simulation of 4- bit full adder using transmission gate shows in fig. 7. It shows the behaviour of 4-bit full adder in full custom design. It also shows the power in terms of milliwatt which is less than semi custom design. Power consumption in full custom design method is 0.180 mW.

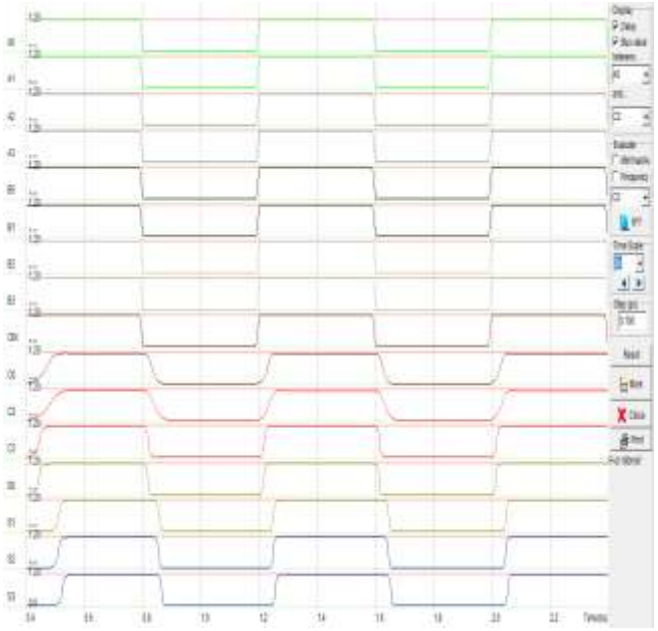

Fig. 7 SPICE Simulation Full Custom design.

V. Result and Discussions

In semi custom design for 4- bit full adder width is 33.4 µm (667 lambda) and height is 26.9 µm (538 lambda). So, the 4-bit full adder has surface area 897.1µm ^{2} . In full custom design for 4- bit full adder width is 29.0 µm (579 lambda) and height is 21.8 µm (436 lambda). So, the 4-bit full adder has surface area 631.1µm ^{2} Table1 shows the comparison between two design methods semi custom design and full custom design.

TABLE 1 Comparison of two design method for their parameters

Parameters	Semi Custom Design	Full Custom Design
Width (µm)	33.4	29.0
Height (µm)	26.9	21.8
Surface Area(µm ^{2})	897.1	631.1
Power (mW)	0.244	0.180

Now full custom design reduces the width from 33.4 µm to 29.0 µm and height reduces from 26.9 µm to 21.8 µm as comparison to semi custom design method. So, full custom design reduces the surface area from 897.1 µm ^{2} to 631.1µm ^{2} . Power consumption in full custom design of 4-bit full adder using transmission gate reduces form 0.244 mW to

0.18 mW as comparison to semi custom design method. Fig. 8 shows the graphical representation of surface area.

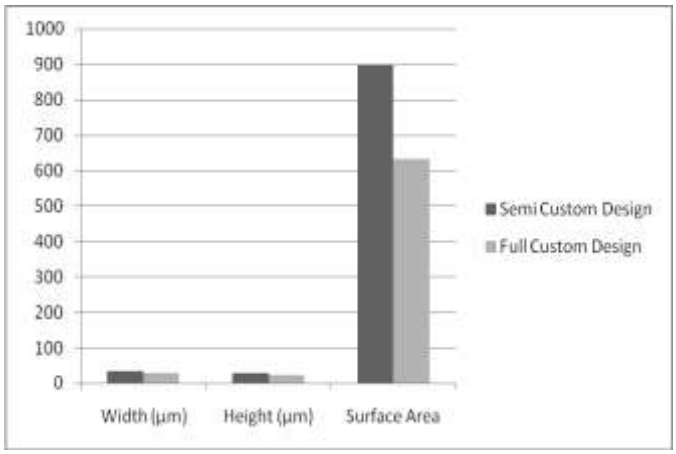

Fig. 8 Graphical comparison of different parameters for 4- bit full adder.

Fig. 9 shows the power parameter of the two design method. It shows the power in milliWatt for both semicustom design method and fully custom design method.

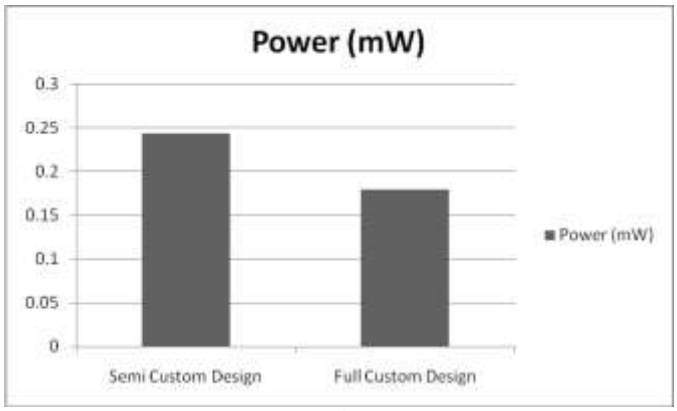

Fig. 9 Graphical comparison of power between two methods.

So, the full custom design method is better than semicustom design method due to it provides the same logic with reduce in both surface area and power consumed in 4-bit full adder using transmission gates.

VI. Conclusions

In this paper 4- bit full adder using transmission gate is designed with two design methods. These are semi custom design method and full custom design method. Transmission gate is used to strength low logic and high logic signal. It improves the degradation in signal logic level. After comparison of parameters width, height and surface area. Full custom design reduces silicon surface area from 897.1µm^2 to 631.1µm^2 as compare to semi custom design method. This is basically due to use of reduced transistor's width. N-well is also used to reduce silicon surface area. Power is also reduced in fully custom design method from 0.244mW to 0.18 mW. After comparing two design methods. It has been found that full custom design method reduces both surface area and power consumption of 4-bit full adder using transmission gate. Simulation of 4-bit full adder using transmission gate is found with 90nm technology. So, it has been found that full custom design method is better than semi custom design method.

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