

Integer N Frequency Synthesizer using Phase Lock Loop

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Abstract— A new architecture and simulation of an integer n frequency synthesizer using PLL for RF application has been illustrated in this paper. This design consists of low power phase frequency detector, low jitter charge pump, ring oscillator based VCO, passive loop filter and 8 bit frequency divider using 250nm technology. This presents the simplest way to design and simulate integer n frequency synthesizer and lock the PLL. The design and analysis of PLL is done on simulation EDA TANNER TOOL 13.0. The main benefit of using PLL technique in Frequency Synthesizer is that it can generate frequencies of 100-200MHz comparable to the accuracy of a crystal oscillator. This paper gives a brief introduction to the basics of Phase Locked loops.

Keywords — Phase locked loop, Phase frequency detector, Charge pump, Loop filter, Voltage controlled oscillator, Frequency divider.

I. INTRODUCTION

Phase Lock Loop (PLL) is a new class of circuit, used primarily in communication applications. It is suitable for a wide variety of applications, such as AM radio receivers, frequency demodulators, multipliers, dividers and as frequency synthesizers. The first Phase Lock Loop ICs came in existence around 1965, and was built using purely analog devices. Recent advances in integrated circuit design techniques have led to an increased use of the PLL as it has become more economical and reliable. Now a whole circuit can be integrated as a part of a larger circuit on a single chip. This paper gives a brief introduction to the basics of PLL. PLL is the most constituent of modern electronics system. A Phase Lock Loop is a negative feedback system that locks reference signal with feedback signal.[1]

• Phase Locked Loop Fundamentals

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL tracks the phase changes that are within the bandwidth of the PLL. A PLL is a negative feedback control system circuit. As the name implies, the purpose of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is done after many iterations of comparing the reference and feedback signals. The

overall goal of the PLL is to match the reference and feedback signals in phase, this is the lock mode. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant. [6]

A basic form of PLL consists of five main blocks:

1. Phase Frequency Detector (PFD)
2. Charge Pump (CP)
3. Low Pass Filter (LPF)
4. Voltage Controlled Oscillator (VCO)
5. Frequency Divider

A PLL is a device which causes a signal to track another one. It keeps an output signal synchronizing with a reference signal input signal as well as in phase. More precisely, the PLL is simply a servo system, which controls the phase of its output signal in such a way that the phase error between output phase and reference phase reduces to a minimum. [(2),(3)]

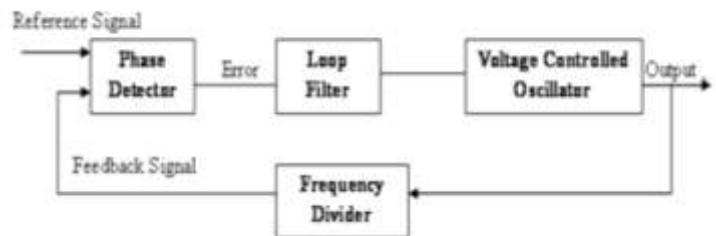


Fig (1) Block diagram of Phase Locked Loop

The phase detector compares the phase of the output signal to the phase of the reference signal. If there is a phase difference between the two signals, it generates an output voltage, which is proportional to the phase error of the two signals. This output voltage passes through the loop filter and then as an input to the voltage Controlled oscillator (VCO) controls the output frequency. Due to this self correcting technique, the output signal will be in phase with the reference signal. When both signals are synchronized the PLL is said to be in lock condition. The phase error between the two signals is zero or almost zero at this.

As long as the initial difference between the input signal and the VCO is not too big, the PLL eventually locks onto the input signal. This period of frequency acquisition, is referred as pull-in time, this can be very long or very short, depending on the bandwidth of the PLL. The bandwidth of a PLL depends on the

characteristics of the phase detector (PD), voltage controlled oscillator and on the loop filter. Before going to look at overall loop operation, let us discuss the main functional blocks in some more detail.[4]

1) Phase Frequency Detector

The very first block of PLL is Phase Detector. The role of Phase Detector/comparator in a phase-locked loop circuit is to provide an error signal which is some function of the phase error between the input signal and the VCO output signal [4]

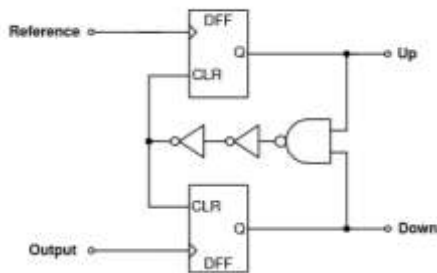


Fig (2) Phase Frequency Detector

PFD is a device which compares the phase of two input signals and provides a signal in the form of phase error. It has two inputs which correspond to two different input signals, usually one from a current starved voltage controlled oscillator and other is a reference source. It has two outputs which instruct subsequent circuitry on how to adjust to lock onto the phase.

From Fig the Schematic Circuit of Phase Frequency Detector compares the leading edges of data and data1 (data is the input signal to PFD, data1 is considered as the feedback signal from the output of VCO to PFD). A data1 rising edge cannot be present without a data rising edge. If the rising edge of the data leads the data1 rising edge, the "Up" output of the phase detector goes high while the "Down" output remains low. [5] This causes the data1 frequency to increase and makes the edges move closer. If the data1 signal leads the data, "Up" remains low while the "Down" goes high. And we can find the phase difference between data1 and data.

2) Charge Pump

A charge pump circuit is used to convert the digital signal from the phase frequency detector to analog signal, the output of which is used to control the frequency of the voltage control oscillator. The output of the PFD should be combined into a single output to drive the loop filter. In Fig (3) Charge pump, two NMOS and two PMOS are connected serially. The uppermost PMOS and lowermost NMOS are considered as the current source and the other PMOS and NMOS in the middle are connected to the "Up" and "Down" of the output of PFD, respectively. When the PFD "Up" signal goes high, the PMOS will turn on. This will connect the current source to the loop filter.

It is in the similar way when the PFD "Down" signal goes high.

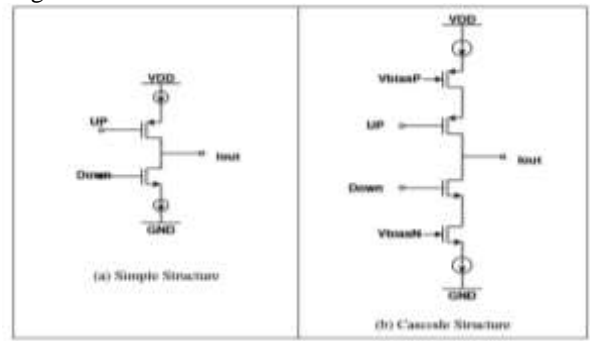


Fig (3) Charge Pump Structure

3) Loop Filter

Filters are frequently added after the charge pump to reduce the ripple. The function of the loop filter is to convert the output signal of phase frequency detector to control voltage and also to filter out any high frequency noise introduced by the PFD.[(10),(11)] The loop filter shown in Fig used with this type of PFD is a simple RC low-pass filter.

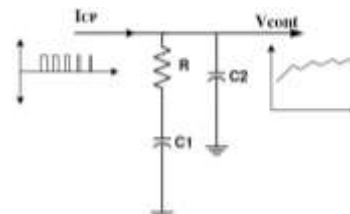


Fig (4) Loop Filter

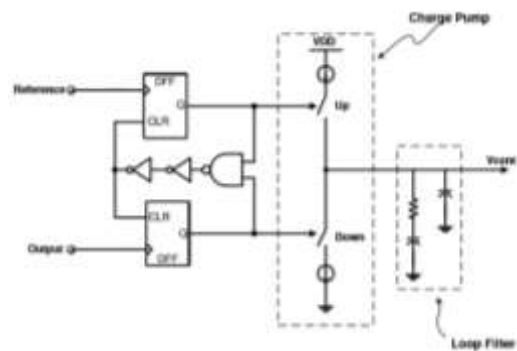


Fig (5) PFD, Charge Pump and Loop Filter

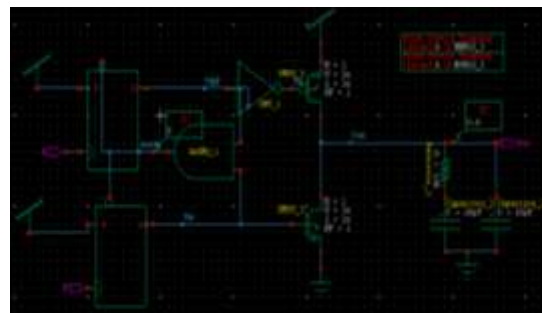


Fig (6) Schematic diagram of PFD, Charge Pump and Loop Filter

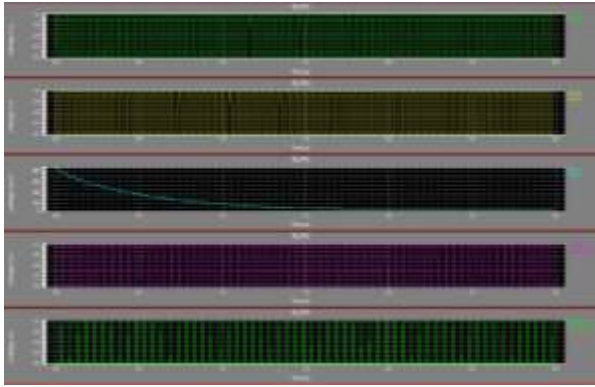
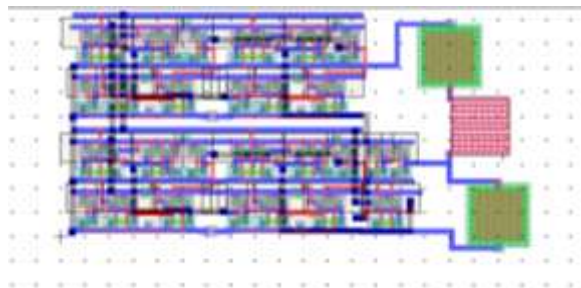


Fig (7) Output waveform of PFD, Charge pump & Loop Filter



Fig(8) Layout of PFD

4) Voltage controlled Oscillator (VCO)

A VCO is a voltage controlled oscillator, whose output frequency ω_0 is linearly proportional to the control voltage v_c generated by the Phase detector. This linear relation between the control voltage and the output frequency simplifies the PLL design. Here we used a ring oscillator VCO.

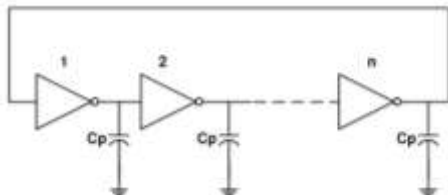


Fig (8) Ring Oscillator

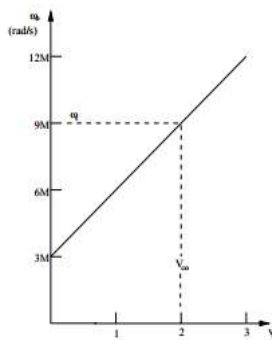


Fig (9) VCO characteristic

The slope of the curve is constant. As the v_c varies from 0 to 2 volts, the output frequency of the VCO varies from 3 Mrad/s to 12 Mrad/s. Outside this range the curve may not be linear and the VCO performance degrades or become non-linear. Depending on the specific requirements of a circuit, the range can be

selected such that the circuit always remains in its linear range, so the non-linear range is not an issue here. When the PLL is in the lock condition, the output frequency $\omega_0 = \omega_i$.

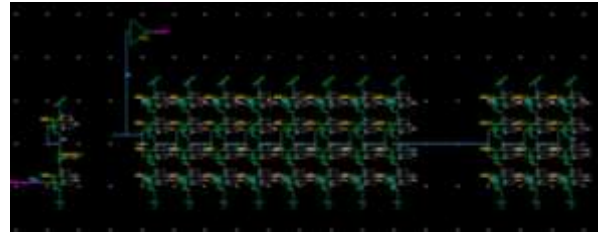
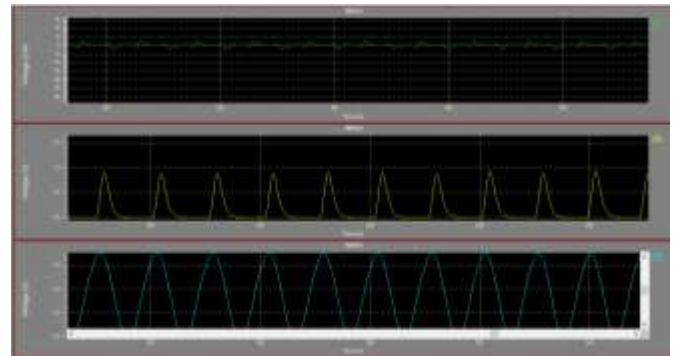


Fig (10) Schematic diagram of Ring Oscillator



Fig(11) Output waveform of VCO

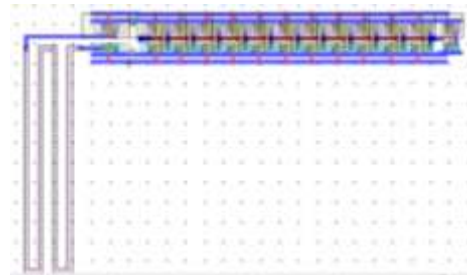


Fig (12) Layout of Ring VCO

5) Frequency Divider

Besides a PLL it also includes a very stable crystal oscillator with a divide by N programmable divider in the feedback loop. The programmable divider divides the output of the VCO by N and locks to the reference frequency generated by a crystal oscillator.

Frequency divider divides the VCO frequency to generate a frequency which is comparable with reference frequency. Here we used divide by N network, we can vary the divider network for synthesis of different frequencies. It divides the clock signal of VCO and generates clock as shown in Fig then applied to phase frequency detector which compare it with input data [8].

The operation of the programmable divide-by-N counter can be described as follows. The number of divide-by-two counter is the number of bits needed to represent the largest loop divider number. The programmable input is represented in binary number as $B_n B_{n-1} \dots B_1 B_0$. The output of all such counters is fed to an end-of-counter (EOC) detector. The counter

counts down from a certain given number, N, until it reaches zero. When the counter reaches zero, the EOCB is the invert of EOC and it signals a reset circuit to initialize the counter back to N (fig 13)

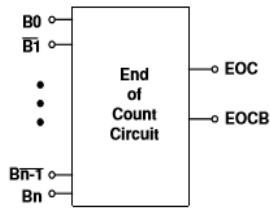


Fig (13) n-bit programmable counter

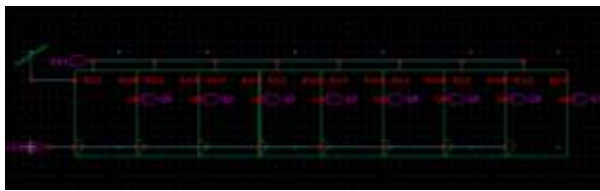


Fig (14) Schematic Diagram of 8-bit counter

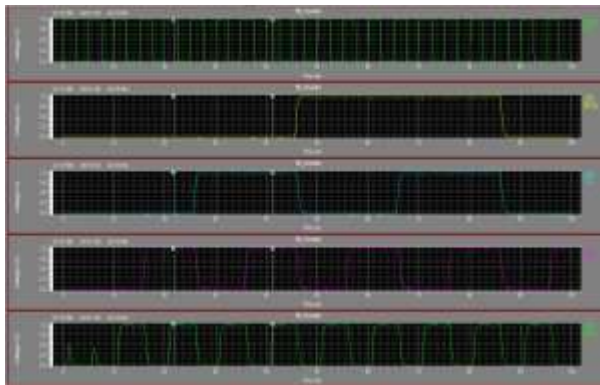


Fig (15) output waveform of counter



Fig (16) Layout of feedback loop

• **Integer N Frequency Synthesizer using PLL**

Thus the final circuit comprises of all the above discussed blocks .As it is earlier described that the integer n frequency synthesizer using Phase Lock Loop here made by using PFD ,Charge pump ,Loop Filter, Starved ring VCO and an 8-bit counter in the feedback loop.[12] Here presented the systematic representation of the overall system.

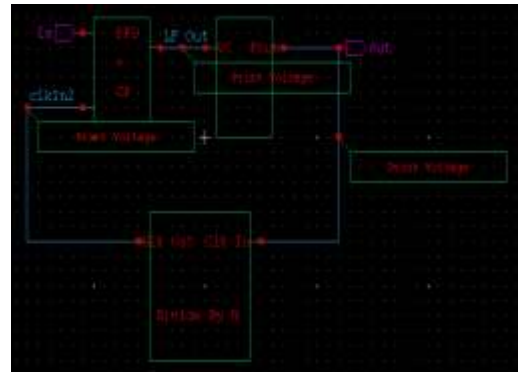


Fig (17) Integer N Frequency Synthesizer using PLL

The simulated result of schematic is viewed on the W (waveform)-edit of the Tanner tool.The final output waveform of complete Integer N Frequency Synthesizer using Phase Lock Loop is shown in fig (18).

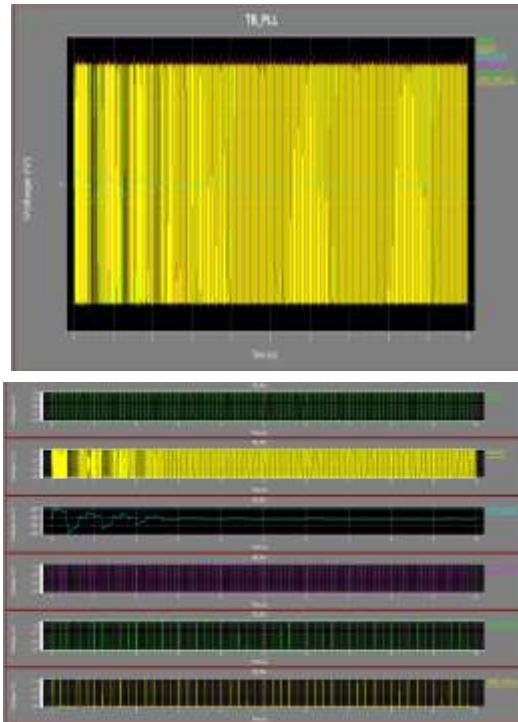


Fig (18) output waveform of final circuit

The above output consists of following signals:

- IN is for one of the input signal
- PFD Up is for output of PFD Up signal.
- PFD Dn is for output of PFD down signal.
- LF out is the output of Loop Filter
- clkIN is the output of VCO.
- ClkOUT is the output of Divider circuit, this performing divide by 8 operations.

- ClkIN2 is the second input to the PFD and the output of divider circuit too.

II. RESULTS AND DISCUSSION

The subject of Phase Lock Loop is wide and diverse. There are many other aspects that can be combined in the design to achieve better performance and more powerful results. The PLL for high performance and RF application has been designed using 250nm CMOS technology and simulated on EDA TANNER 13.0. The proposed VCO has been designed for getting optimized 100-200MHz frequency, average power consumption of 3.6734e-004W and supply voltage of 1.2volt. Since the area calculated is the sum of areas of individual circuits of the PLL because it was complex for me to make the layout of the whole system, this will be completed as my future work.

S.No.	Parameters	250nm Technology
1	Tool	TANNAER 13.0
2	Supply Voltage	1.2V
3	Power Consumption	3.6734e-004W
4	Maximum Power	1.082866e-003W
5	Minimum Power	7.320522e-005W
6	Area	43.924 μm ²
7	Reference Frequency	5MHz
8	Output Frequency	100-200MHz
9	Charge Pump Current	27 μA
10	Series Resistance	10K
11	Series Capacitance	20pF
12	Parallel Capacitance	20pF
13	Gate length	0.25
14	Control Voltage	1.8V

Table 1: Output of Integer N Frequency Synthesizer using PLL

Comparative study of results

The results are compared with the following research papers and the current study of PLL. They are summarized as follows:

S.No.	Parameters	My Design	[6]	[9]	[15]
1	Tool	Technology TANNER 13.0			
2	Technology	250nm	350nm	180nm	250nm
3	Power Supply	1.2V	3.0V	0-2V	2.5V
4	Reference frequency	5MHz	20MHz	5MHz	70MHz

			2GHz		
5	Output Frequency	100-200MHz	350MHz-16GHz	5.15-5.25GHz	180-320MHz
6	Gate Length	0.25	0.35	0.18	0.25
7	Power consumption	3.6734e-004W	7.6mW	-	3.875mW
8	Area	43.924 μm ²	-	-	45.666 μm ²
9	Charge Pump Current	27 μA	20 μA	125 μA	-
10	Series Resistance	10K	18K	276.125K	-
11	Series Capacitance	20pF	24pF	9.22pF	
12	Parallel Capacitance	20pF	3pF	0.61pF	

Table 2 Comparative Results of PLL

III. CONCLUSIONS

The design of PLL based integer type frequency synthesizers for wireless transceivers involves the compliance with a defined set of specifications. Phase locked loop remained an interesting topic for the research, as it covered many discipline of electrical engineering such as Communication Theory, Control Theory, Signal Analysis, Design with transistors and op amps, Digital circuit design and non-linear analysis. The PLL has been designed with low power, small chip size using 250nm CMOS technology for high performance PLL and simulated by EDA TANNER TOOL 13.0.

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REFERENCES

- [1] Neil H.E.Weste and David Money Harris "CMOS VLSI – A Circuits and Systems Perspective Fourth edition"
- [2] R.J.Baker, H.W.Li, and D.E.Boyce, "CMOS Circuit Design, Layout, and Simulation," IEEE Press Series on Microelectronic Systems, 2002.
- [3] Gayathri M G* "Design of All Digital Phase Locked Loop in VHDL" Gayathri M G / International Journal of Engineering Research and Applications (IJERA) ISSN:

- 2248-9 www.ijera.com Vol. 3, Issue 4, Jul-Aug 2013, pp.1074-1076
- [4] W. Alan Davis, Krishna Agarwal "Radio Frequency Circuit Design" Copyright © 2001 John Wiley & Sons, Inc. Print ISBN 0-471-35052-4 Electronic ISBN 0-471-20068-9
- [5] *General PLL Description: T. H. Lee, Chap. 15. Gray and Meyer, 10.4 Clock generation: B. Razavi, Design of Analog CMOS Integrated Circuits, Chap. 15, McGraw-Hill, 2001.*
- [6] Vemula Lohith Kumar¹ IBTech Student, School of Electronics, Vignan University, Vadlamudi, Guntur, AP, India 'Simulation of Integer N Frequency Synthesizer' *International Journal of Engineering Trends and Technology (IJETT) - Volume4 Issue6- June 2013*
- [7] Kanika Garg, ACSD Department, CDAC1; V.Sulochana Verma, ACSD Department, CDAC2 "DESIGN OF LOW POWER PHASE LOCKED LOOP IN SUBMICRON TECHNOLOGY" *International Journal of Advanced Technology & Engineering Research (IJATER)*
- [8] Yashpal Sen¹ and Nitin Jain² *1M.Tech. Scholar, Dept. of ET&T (Digital Electronics) C.E.C., Bilaspur, CSVTU, (C.G.), INDIA. 2Dept. of E&TC, C.E.C., Bilaspur, CSVTU, (C.G.), INDIA. "Design and Implementation of Phase Locked Loop Using Current Starved Voltage Controlled Oscillator" Advance in Electronic and Electric Engineering. ISSN 2231-1297, Volume 4, Number 6 (2014), pp. 637-644 © Research India Publications <http://www.ripublication.com/aeee.htm>*
- [9] K.Rajasekhar, S.Adilakshmi, T.B.K. Manoj kumar "Design of High Performance Phase Locked loop for Multiple outputs with Ultra Low Power Sub Threshold Logic" *International Journal of Engineering Research and Applications (IJERA)* ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 2,Mar-Apr 2012, pp.046-052
- [10] Jyoti P. Patra and Umesh C. Pati "Behavioural Modelling and Simulation of PLL Based Integer N Frequency Synthesizer using Simulink" *International Journal of Electronics and Communication Engineering. ISSN 0974-2166 Volume 5, Number 3 (2012), pp. 351-362 © International Research Publication House <http://www.irphouse.com>*
- [11] Dr. P.H.Tandel, Anuradha P. Garge "Design of General Order Digital Phase Locked Loop" *International Journal of Engineering and Innovative Technology (IJEIT) Volume 2, Issue 7, January 2013*
- [12] Abhilasha N.S "Optimized Design of Digital Phase Locked Loops for RF Carrier Acquisition" *IJSRT (INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY) ISSN: 2277-9655 Scientific Journal Impact Factor: 3.449 (ISRA), Impact Factor: 1.85,1,May2014*
- [13] Varsha Prasad¹, Dr Chirag Sharma² "A Review of Phase Locked Loop" *International Journal of Emerging Technology and Advanced Engineering Website: www.ijetae.com (ISSN 2250-2459, Volume 2, Issue 6, June 2012)*
- [14] Guan- Chyun Hsieh, senior member,IEEE, and James C.Hung,Fellow,IEEE "Phase- Locked Loop Techniques- A Survey" *IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL.43,NO.6,DECEMBER 1996*
- [15] Anitha Babu, Bhavya Daya, Banu Nagasundaram, Nivetha Veluchamy "All Digital Phase Locked Loop Design and Implementation" *University of Florida, Gainesville, FL, 32608, USA*
- [16] Curtis Barret "Fractional/Integer-N PLL Basics" *Technical Brief SWRA029*
- [17] B .Razvi, "Design of ANALOG CMOS Integrated Circuits" *McGraw- Hill, 2001.*
- [18] K. Shu, E. Sanchez-Sinencio, J. Silva-Martinez, and S.H.K. Embabi, "A 2.4-GHz monolithic fractional-N frequency synthesizer with robust phase-switching prescaler and loop capacitance multiplier", *IEEE Journal of Solid-State Circuits, vol. 38, no. 6, pp. 866-874, June 2003.*
- [19] Volodymyr Kratyuk, Pavan Kumar Hanumolu, Un-Ku Moon, and Kartikeya Mayaram, "A Design Procedure for All-Digital Phase-Locked Loops Based on a Charge-Pump Phase-Locked-Loop Analogy" *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 54, NO. 3, MARCH 2007*
- [20] Kusum Lata and Manoj Kumar "ALL Digital Phase-Locked Loop (ADPLL): A Survey" *International Journal of Future Computer and Communication, Vol. 2, No. 6, December 2013*