Capacitance Scaling Based Low Power Comparator Design on 28nm FPGA

Abhay Saxena[#1], Swapnil Gaidhani[#2], Anamika Pant[#3] Chandrashekhar Patel[#4]

[#1,2,4] *Department of Computer science DSVV India*
[#3] *Department of Computer science Kumaon University India*

Abstract— *Reducing the power consumption is the main concern in green computing. So here we used capacitance scaling technique on comparator for optimizing the power. We worked with I/O Power & Leakage Power because Clock Power & Signal Power are independent of capacitance scaling. In our work we have scaled down the capacitance from 512pF to 32pF at various fixed frequency. At 1GHz when we scale down the capacitance from 512pF to 32pF then we got 91.26% reduction in total I/O power dissipation. At 10 GHz when we scale down the capacitance from 512pF to 32pF then we got 91.36% reduction in total I/O power dissipation. At 20 GHz when we scale down the capacitance from 512pF to 32pF then we got 91.364% reduction in total I/O power dissipation. At 30 GHz when we scale down the capacitance from 512pF to 32pF then we got 91.3624% reduction in total I/O power dissipation. At 40GHz when we scale down the capacitance from 512pF to 32pF then we got 91.36277% reduction in total I/O power dissipation. This design is implemented on 28 nm Artix7 FPGA.*

Keywords — *Capacitance Scaling, Low Power, Comparator, 28nm, FPGA, Computer Architecture*

I. INTRODUCTION

In the area of Computer Science and Electronics, **comparator** is an essential component in computer system architecture which compares two analog voltages or currents and produce an output as a digital signal indicating which is larger.

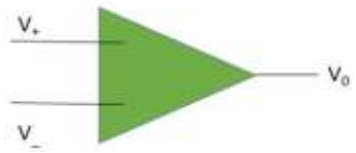

Figure 1: Comparator

In figure 1 we have two analog input terminal V_+, V_- and one output V_0 as one bit digital signal, In practical environment following rules followed by comparator output

- If $V_+ > V_-$ then output bit is one.
- If $V_+ < V_-$ then output bit is zero.

We have designed our own comparator where we have two analog input terminals (A, B both are 8-bits) and also have one selection line (S of 3 bits) and a one single clock. The output is ideally which is one binary digital output(Y of single bit) as shown in figure 2 and figure 3.

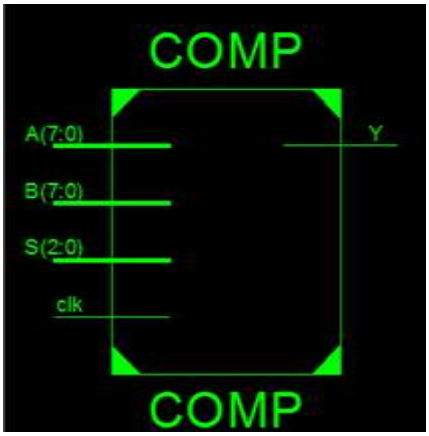

Fig.2: Top Level Schematic of 8-bit Comparator.

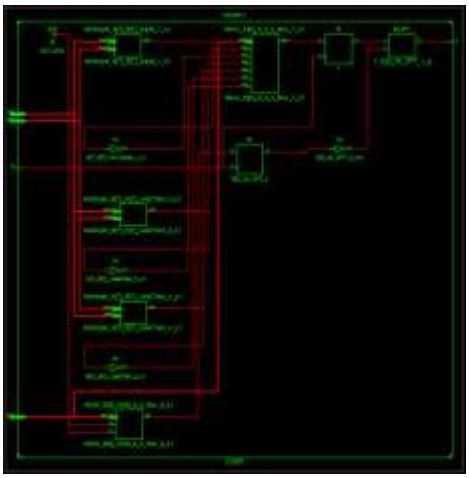

Figure 3: RTL Schematic of a 32 bit Comparator.

II. Literature Survey

Capacitance scaling was used for energy efficient design of ALU [1, 7], FIR filter [2], Unicode reader [3, 6], image inverter [4], register [5], and UART [8]. Energy efficient 64-bit arithmetic logic unit (ALU)

design is operating in a wide range of frequencies and capacitance [1]. Energy efficient FIR filter also helpful in saving of power when used for digital signal processing [2]. Capacitance scaling and frequency scaling were done in order to make energy efficient Image Inverter design [4]. Capacitance scaling was implemented in register to optimize the power dissipation [5]. Researcher scale down the output load capacitance value from 5555pF to 555pF, 55pF, and 5pF and achieve around 90% saving in power dissipation [7]. In [8], they achieved 99.72% reduction in IOs power consumption of Universal Asynchronous Receiver Transmitter (UART) when they scale down output load from 10,000pf to 5pF in IOB setting of FPGA [8]. HSTL IO Standards Based Processor Specific Green Counter [9]. Leakage Power Reduction with Various IO Standards and Dynamic Voltage Scaling in Vedic Multiplier on Virtex-6 FPGA [10]. High Performance FIFO Design for Processor through Voltage Scaling Technique[11].

III. Power Analysis of Capacitor on Airtex-7 FPGA

Here have taken two parameter in our work first is capacitance and second is frequency. We have scaled down the capacitance value from 512pF to 32pF at different – different fixed frequency and calculate the change in dynamic power.

Figure: 4

Total power is equal to sum of dynamic and static power as shown in figure 4.

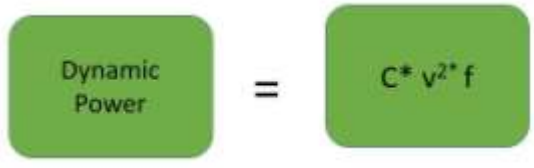

Figure: 5

Dynamic power is directly proportional to capacitance and frequency as shown in figure 5, means if we scale down the frequency and capacitance value then there will be reduction in total power.

Table 1

Power Consumption at 1 GHz Frequency

Power (in Watts) Capacitance	Clock Power	Leakage Power	Signal Power	I/O Power
512 pF	0.008	0.104	0.001	1.122
256 pF	0.008	0.101	0.001	0.576
128 pF	0.008	0.009	0.001	0.303
64 pF	0.008	0.098	0.001	0.166
32 pF	0.008	0.098	0.001	0.098

In table 1 we have done our power consumption analysis of a Comparator at **1GHz** frequency. When we change the capacitance from 512 pF to 32 pF then then we got 91.26% reduction in total I/O power and 5.76% in leakage power. We have also converted our tabular data into bar graph for better analysis as shown in figure 6.

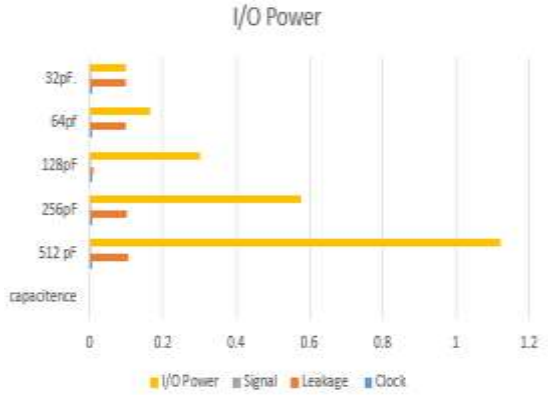

Figure: 6 I/O Power consumption at 1 GHz

Table 2
Power Consumption at 10 GHz Frequency

Power (in Watts) Capacitance	Clock Power	Leakage Power	Signal Power	I/O Power
512 pF	0.083	0.348	0.01	17.022
256 pF	0.083	0.172	0.01	8.728
128 pF	0.083	0.128	0.01	4.581
64 pF	0.083	0.113	0.01	2.507
32 pF	0.083	0.106	0.01	1.47

In table 2 we have done our power consumption analysis of a Comparator at **10GHz** frequency.

When we change the capacitance from 512 pF to 256 pF then there is 48.72% reduction in total I/O power and 50.57% reduction in leakage power. Once we decrease the capacitance further to128 pF then we got 73.08% reduction in total I/O power and 63.21% reduction in leakage power. Going further with 512pF to 64 pF we reduced the total I/O power to 85.27% and leakage power to 67.52%. In last when we scale down the capacitance from 512pF to 32 pF then there is 91.36% reduction in total I/O power dissipation and 69.54% reduction in leakage power. We have also converted our tabular data into bar graph for better analysis as shown in figure 7.

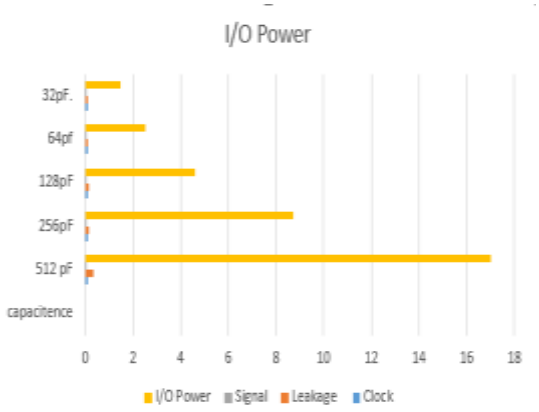

Figure: 7 I/O Power consumption at 10 GHz

Table 3

Power Consumption at 20 GHz Frequency

Power (in Watts) Capacitance	Clock Power	Leakage Power	Signal Power	I/o Power
512 pF	0.166	1.614	0.019	34.044
256 pF	0.166	0.365	0.019	17.456
128 pF	0.166	0.179	0.019	9.161
64 pF	0.166	0.132	0.019	5.014
32 pF	0.166	0.116	0.019	2.94

In table 3 we have done our power consumption analysis of a Comparator at **20GHz** frequency. When we change the capacitance from 512 pF to 256 pF then there is 48.02% reduction in total I/O power and 77.38% reduction in leakage power. Once we decrease the capacitance further to128 pF then we got 73.09% reduction in total I/O power and 88.90% reduction in leakage power. Going further with 512pF to 64 pF we reduced the total I/O power to 85.27% and leakage power to 91.82%. In last when we scale down the capacitance from 512pF to 32 pF then there is 91.364% reduction in total I/O power dissipation and 92.81% reduction in leakage power dissipation. . We have also converted our tabular data into bar graph for better analysis as shown in figure 8.

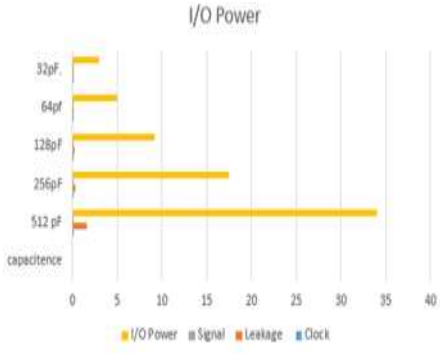

Figure: 8 I/O Power consumption at 20 GHz

Table 4

Power Consumption at 30 GHz Frequency

Power (in Watts) Capacitance	Clock Power	Leakage Power	Signal Power	I/O Power
512 pF	0.248	2.309	0.029	51.067
256 pF	0.248	0.816	0.029	26.183
128 pF	0.248	0.248	0.029	13.742
64 pF	0.248	0.159	0.029	7.521
32 pF	0.248	0.128	0.029	4.411

In table 4 we have done our power consumption analysis of a Comparator at **40GHz** frequency. When we change the capacitance from 512 pF to 256 pF then there is 48.72% reduction in total I/O power and 64.66% reduction in leakage power. Once we decrease the capacitance further to128 pF then we got 73.09% reduction in total I/O power and 89.25% reduction in leakage power. Going further with 512pF to 64 pF we reduced the total I/O power to 85.27% and leakage power to 93.11%. In last when we scale down the capacitance from 512pF to 32 pF then there is 91.36277% reduction in total I/O power dissipation and 94.45% reduction in leakage power . We have also converted our tabular data into bar graph for better analysis as shown in figure 9.

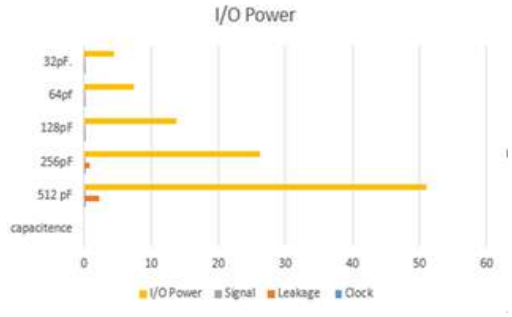

Table 5

Power Consumption at 40 GHz Frequency

Power (in Watts) Capacitance	Clock Power	Leakage Power	Signal Power	I/o Power
512 pF	0.331	2.309	0.038	68.089
256 pF	0.331	1.766	0.038	34.911
128 pF	0.331	0.402	0.038	18.322
64 pF	0.331	0.195	0.038	10.028
32 pF	0.331	0.142	0.038	5.881

In table 5 we have done our power consumption analysis of a Comparator at **40GHz** frequency. When we change the capacitance from 512 pF to 256 pF then there is 48.72% reduction in total I/O power and 23.51% reduction in leakage power. Once we decrease the capacitance further to128 pF then we got 73.09% reduction in total I/O power and 82.58% reduction in leakage power. Going further with 512pF to 64 pF we reduced the total I/O power to 85.27% and leakage power to 91.55%. In last when we scale down the capacitance from 512pF to 32 pF then there is 91.36277% reduction in total I/O power dissipation and 93.85% reduction in leakage power. We have also converted our tabular data into bar graph for better analysis as shown in figure 10.

Figure: 10 I/O Power consumption at 40 GHz

IV. Conclusion

We have designed our 8 bit comparator with serial input and output pattern and applied capacitance scaling technique for less I/O power consumption. In this paper researcher take different –different frequency (40 GHz to 1GHz) and scale down the capacitance form 512pF to 32pF.

We have summarized our work through table 6 which is containing information regarding the Leakage Power and total I/O power dissipation at different-different frequency. At last we found that Dynamic power (Leakage Power and I/O Power) is directly proportional to Capacitance and frequency.

Table: 6

Capacitance / Frequency	40GHZ		30GHZ		20GHZ		10GHZ		1GHZ	
	I/O Power	Leakage Power	I/O Power	Leakage Power	I/O Power	Leakage Power	I/O Power	Leakage Power	I/O Power	Leakage Power
512 pF	68.089	2.309	51.067	2.309	34.044	1.614	17.022	0.348	1.122	0.104
256 pF	34.911	1.766	26.183	0.816	17.456	0.365	8.728	0.172	0.576	0.101
128 pF	18.322	0.402	13.742	0.248	9.161	0.179	4.581	0.128	0.303	0.009
64 pF	10.028	0.195	7.521	0.159	5.014	0.132	2.507	0.113	0.166	0.098
32 pF	5.881	0.142	4.411	0.128	2.94	0.116	1.47	0.106	0.098	0.098

V. Future Scope

We design a basic comparator with capacitance scaling to reduce the power consumption of circuit.

If we will talk about to design a processor then we required register, ALU, Control Unit. We can apply the same capacitance scaling technique to all of this components to make a power efficient processor. If we will able to reduce the power consumption of processor then it would be significant for us. This design is implemented on 28nm Artix7 FPGA so there is open scope to redesign this circuit on 28nm Virtex-7,65nm Virtex-5 and 40nm Virtex-6, 90nm Virtex-4 FPGA to achieve further power reduction as well.

VI. Acknowledgment

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