Fault Detection and Test Minimization Methods for Combinational Circuits - A Survey

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***Abstract*— Rapid increase in population increased the usage of digital components dramatically and their production. For profitable income, the cost of the finished product and time taken for marketing the product needs to be reduced. In this paper, the authors conducted extensive survey of methods developed earlier to detect faults and minimize test set in digital circuits. The survey is limited to methods for simple combinational circuits only. In effect, this paper compares 11 different fault detection and test minimization methods for simple circuits. In addition, a survey on evolutionary techniques for optimizing the test set in digital circuits is performed. The surveyed methods are widely accepted by industries manufacturing digital circuits. A very brief introduction to entire flow of test minimization process is also presented.**

***Keywords*— Combinational Circuits, Fault Detection, Genetic Algorithm, ILP, Stuck-at-faults, Test Minimization.**

I. INTRODUCTION

In recent years, the development of integrated circuit technology has accelerated rapidly. VLSI techniques promise to make today's functional level devices and tomorrow's basic components. Accordingly, digital systems are built with more and more complexity; the fault testing and diagnosis of digital circuits becomes an important and indispensable part of the manufacturing process[13].

With the advances in science and technology, modern devices are becoming more and more complex every day. As the device complexity increases, testing becomes even more complex. Circuits are shrinking in physical size while growing both in speed and range of capabilities. This rapid advancement is not without serious problems, however. Especially worrisome are verification and testing, which become more important as the system complexity increases and time-to-market decreases. This results in increased test time and higher test cost[2]. At the same time, the manufacturing cost of a device is reduced due to the higher levels of integration. Hence the necessity of reducing the test cost. To decrease the test cost, the time required to test a device needs to be decreased. So, we simply need to devise a test set that is small in size.

All manufactured VLSI chips are tested for defects. But it is not possible to generate or apply vectors to test all possible defects in a chip. So defects are modeled as faults to ease the test generation process. Among the various existing fault models, the single stuck-at fault model is widely accepted because of its closeness to actual defects and the algorithmic possibilities it offers for generating test vectors[8]. This paper will discuss more on fault detection and test minimization based on stuck-at-fault models. The assumptions about the types of circuits is explained in section 2. The assumptions about the types of faults are discussed in section 3. The section 4 analyzes different fault detection methods that range from fault table method to the latest GA based test minimization method. Section 5 compares the performance of different fault detection methods.

II. TYPES OF CIRCUITS

Types of digital circuits under study are simple two stage combinational circuits. The practical digital circuits, which are composed of AND, OR, NOT, NAND and NOR gates are alone chosen for evaluating the performance of the methods in survey. Furthermore, the methods derived for obtaining tests for this class of circuits are general enough to be applied to circuits consisting of gates other than these five types, such as the XOR gate, with minor modifications. It is assumed that the response delays of all the gate elements are the same. Figure 1 shows an example of a simple two stage combinational circuit. X1,X2 and X3 are the circuit inputs and X1X2+X2X3 is the fault free response of the circuit. Interconnections between the gates are numbered.

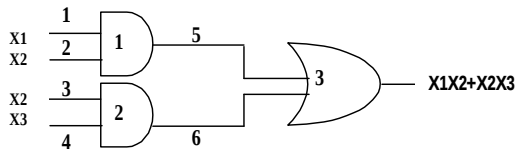

Fig 1. sample circuit

III. TYPES OF FAULTS

The faults considered in this study are assumed to be fixed or permanent or non transient faults, which means that without having them fixed or repaired, the fault will be permanently there. Most of the faults occurring in currently used circuits, such as resistor-transistor logic circuits (RTL) , diode-transistor logic circuits(DTL), and transistor-transistor logic circuits (TTL), are those which cause a wire to be stuck-at-zero(s-a-0) or stuck-at-one(s-a-1). Restricting our consideration to just a class of faults is technically justified[14], since most circuit failures exhibit symptomatically identical effects. This class of faults occur in circuits with discrete components as well as integrated circuits. A multiple fault is defined as the simultaneous occurrence of any possible combination of s-a-0 and s-a-1 faults[3]. This paper discusses fault detection and test minimization based on stuck-at-fault models.

There are some faults in a circuit which are undetectable. A fault of a combinational circuit is said to be detectable if there exists a test by which we can judge whether or not the circuit has such a fault; otherwise, we call the fault undetectable. A combinational circuit is said to be *irredundant* if any logic fault that occurred at any part of the circuit will cause a change in the switching function that the fault-free circuit realizes. All s-a-0 and s-a-1 faults in a circuit are *detectable* if and only if the circuit is irredundant if and only if the function that the circuit realizes is a minimized function[14]. Two faults are said to be *indistinguishable* if the truth tables of the output functions of the circuits with these two faults are completely identical. In other words, we cannot find a test such that the two faults can be distinguished based on the information of the output. If on the other hand, there exists such a test, by applying it the output values of the circuit having the two faults are different; we say that these two faults distinguishable. This paper evaluates the fault detection methods including evolutionary methods spanning over the years mid-1970s to early 2011.

IV. FAULT DETECTION AND TEST MINIMIZATION METHODS

Minimizing test sets is simply termed as test set compaction. Most commonly used method is fault table method. A number of basic analytic and heuristic methods that appeared in the literature[14] includes path sensitizing and Equivalent-Normal-Form(ENF) method, Karnaugh map and tabular method, the ENF karnaugh map method, the Boolean difference method, and the SPOOF method. ILP method and Genetic Algorithm method are used for simple digital circuits.

A. Fixed Scheduled Test Minimization Method

If $x_1, x_2,\ldots..,x_n$ are the input variables to a single output circuit whose fault-free (correct) output is $z = z(x_1,\ldots..x_n)$. $f_1,f_2,\ldots..f_i$ are the erroneous outputs, each corresponding to one of the possible faults $f_1,f_2,\ldots.f_i$. Table I shows fault table F with output combinations for possible input combinations[14] of the chosen circuit. Each corresponding faulty and fault-free outputs are compared using Exclusive-OR operation results $zf_1,zf_2\ldots zf_i$ single bit erroneous outputs shows in fault detection table Table II. The complete test set for any f_i is the set of input combinations $x_j =(x1_j,x2_j \ldots\ldots xn_j)$ such that

$$z(x_j) \oplus zf_i(x_j) = 1 \qquad (1)$$

for all $1\leq i \leq l$, $1\leq j \leq 2^n$

TABLE I. FAULT TABLE

Test No	X_1	X_2	..	X_n	Z	f_1	f_2	…	f_i
1	0	0	..	0	0	1	0	…	0
2	0	0		1	1	1	0	…	1
. . .	. . .	. . .	..	. . .	. . .	. . .	. . .	…	. . .
2^n	1	1	..	1	0	0	0	…	1

TABLE II. FAULT DETECTION TABLE

Test No	X_1	X_2	..	X_n	Z	Zf_1	Zf_2	…	Zf_i
1	0	0	..	0	0	1	0	…	0
2	0	0		1	1	0	1	…	0
. . .	. . .	. . .	..	. . .	. . .	. . .	. . .	…	. . .
2^n	1	1	..	1	0	0	0	…	1

Table II may be simplified as follows. Delete the columns that correspond to undetectable faults. That is, delete the columns zf_i in the table that are identical to z. Combine the columns that correspond to indistinguishable faults. That is, combine the columns zf_i and zf_j if $zf_i = zf_j$. The reduced fault detection table still contains the complete information about the complete test sets for detecting all the detectable faults. In fact, the complete test set for detecting each detectable fault f_i may be obtained by taking Exclusive-OR operations on column zf_i with column z as shown in Equation 1.

In Fixed Scheduled Test Minimization(FSTM) method , the above two tables are generated for the given combinational circuit They are fault table and fault detection table. In fault table 2^n test vectors are generated, where n is the number of inputs present in the circuit. Instead of testing 2^n test vectors, essential test set is found using a new method named as FSTM method. It removes redundancy in test set by grouping test numbers[15], detecting the same fault. Test numbers detecting single faults alone are also collected as essential test numbers.

B. Heuristic Method

In Heuristic Test minimization method, fault table alone is created. A diagnosing tree is created by dissecting the fault diagnostic matrix into two sub matrices based on essential test number. The test number is added to essential test set. Column numbers in these two matrices are added to the root node of the tree as right and left siblings. Left subtree contains fault-free output column numbers from the matrix(0s) and right subtree contains faulty output column numbers from the matrix(1s)[16,17]. The process is repeated until both left and right children results in a single column number in them. Essential test set is found after removing redundant test numbers in nodes.

C. Path Sensitizing Method

This is one of the earliest method used for fault detection. In this method fault detection test may be found by examining the paths of transmission from the location of an assumed fault to one of its primary outputs. This is the principle idea behind the path sensitizing method[14]. The path-sensitizing method is very attractive from the point of view of not requiring the construction of the fault table and is useful for the fault detection of tree like circuits. But for general non-tree like circuits, the process of exhausting all possible single paths, then all possible pair of paths, then all possible groups of three paths and so on, involves quite a lot of searching and computation, even when done by a computer. When fan-out exists, there occurs the additional problem of sensitizing a set of paths which in fact contain all connections. It would be desirable if such tests could be found by direct inspection of the circuit. Unfortunately no such direct technique has been discovered.

D. Equivalent-Normal-Form Method

The *Equivalent Normal Form*(ENF) of a circuit is obtained by expressing the output of each gate as a sum-of-products expression of its inputs and preserving the identity of each gate by a suitable subscript. Each subscripted input variable in a ENF is called literal. An appearance of a literal in a term is also called a literal. An equivalent normal form corresponds to a two-level AND-OR circuit. Consequently, the techniques developed earlier for two-level circuits can now be applied, with several modifications, to the equivalent normal forms. Two major differences, however, exist between these two types of circuits. In the AND-OR circuit each literal corresponds to a circuit input and to a unique path from that input to the circuit output[10]. On the other hand, in the equivalent normal form two variables may have different subscripts because they are associated with two different paths, although they correspond to the same input in the original multilevel circuit.

Path sensitizing method and Equivalent-normal-form method are both based on the concept of path sensitizing. ENF method has several advantages[14] over Path sensitizing method. The ENF method is an analytical method that provides a vehicle for systematically finding the most desirable tests, those which each detect many faults in the circuit. Single paths that are not sensitizable are usually easily seen from the ENF. For instance, when both a variable x and its complement $\bar{x}$ are contained in the same term of an ENF, it indicates that the paths represented by the corresponding two literals of x and $\bar{x}$ cannot be sensitized. Thus these literals cannot be tested for either s-a-0 or s-a-1 fault. The reason for this is that due to reconvergent fan-out, no matter how to sensitize(i.e to sensitize) one of the two paths or both paths simultaneously, the s-a-0 or s-a-1 fault, a contradiction will always result. Another example is that when two or more literals pertaining to the same input variable are contained in the same term, the s-a-1 test for testing either of the literals individually is impossible. The way to derive tests using the ENF is very simple

E. Two- Level- Circuit Fault Detection

The previous methods of construction of a complete fault-detection test set for a combinational circuit using the two basic approaches. First approach is to examine each “individual fault”(the fault-table method). Second approach is to examine each “path”(the path sensitizing method and the ENF method). A third approach to the problem is instead of examining each individual fault or each path, it is proposed to examine each gate of the circuit[14]. A very simple and direct method for constructing a minimal complete fault-detection test set for any two-level AND-OR(OR-AND,NAND-OR,etc) irredundant circuit using this approach is presented.

This method may be considered to have two versions - a graphical and a tabular. The graphical version will first be presented which uses the Karnaugh map, hence is convenient to apply to circuits with a small number of input variables, say not more than six, but preferably not more than four. Then, just as what was done in the minimization of switching functions, this Karnaugh map version is extended to a tabular method in a similar manner as that of Quine-McCluskey. It uses exactly the same principles but without maps, allows the circuit to have any finite number of input variables, and hence is particularly attractive from a machine-computation point of view. First we present the graphical version of this method to two-level AND-OR circuits with input variables not greater than four.

1) Karnaugh Map Method

Karnaugh map technique for test derivation is discussed by L.W.Bearnson and C.C.Carroll [6].The purpose of this method is to develop a map technique from [9] and [13]. At first, minimum two-level sum-of-products will be considered. Factored forms of these expressions will also be investigated, but in all cases the assumption will be made that no redundancy is present in the circuit.

The procedure just outlined for the determination of the set of tests in a fault detection experiment suffers from the limitation inherent in any operation with a map. It is very useful for circuits with a small number of variables, and becomes complicated when the number of variables increases[10]. To overcome this difficulty, the tabular method can be used.

2) Tabular method

Tabular method consists of three steps. First step is the determination of a minimal complete s-a-0 test set T_0. Second step is the determination of a minimal complete s-a-1 test set T_1. Third part is the minimal complete s-a-0 and s-a-1 test set T is the union of T_0 and T_1. It is one of the two level circuit fault detection method and it is used for any number of variables. This method uses exactly the same principles of Karnaugh map method but without maps. It allows the circuit to have any finite number of input variables.

F. Multilevel-circuit Fault Detection

The problem of detecting faults in multilevel circuits is considerably more complicated than in the case of two-level circuits. Except in the case where each gate has only a fan out of 1, it is no longer true that testing only the inputs will always detect all the faults within the circuit. If we try to apply an experiment designed for a two-level circuit to a logically equivalent multilevel circuit in which two or more paths emanate from a certain gate and reconverge at a level closer to the output terminal. A fault in one path may not always be detectable if the other path is faultless[10]. It shall be concerned with procedures for the detection of single faults. This limitation does not, of course, exclude the detection of most double and other multiple faults, but it emphasizes that only single faults will be detected in all cases, while some multiple faults may not be detected.

The design of fault-detection experiments for multilevel combinational circuits is based on the ideas of "path sensitization" and "equivalent normal form," introduced by Armstrong in [4]. Armstrong proved that a set of fault-detection tests devised for the equivalent normal form is also a valid set of tests for the original circuit[10]. Thus the problem of designing experiments for multilevel circuits is equivalent to the design of experiments for the two-level equivalent normal forms.

The minimum sum-of-products or the minimum product-of-sums form of a Boolean expression is not always the most economical to implement. Consequently, a common term or terms is often factored, with the result that a cheaper realization is obtained. AND-OR circuits that realize factored forms are multilevel AND-OR circuits. The purpose of this method is to extend the previous fault-detection methods for two-level AND-OR circuits to this class of multilevel circuits. The circuits considered are again assumed to be irredundant.

G. ENF- Karnaugh map Method

This method is the combination of ENF method and Karnaugh map method. In this method, a Karnaugh map technique for deriving a fault-detection experiment for multilevel circuits, which will give the same result as that obtained by the ENF method[14]. It is much simpler technique than the ENF method, as it does not use a scoring technique and is without the complemented ENF. An ENF corresponds to a two level AND-OR circuit. Consequently, the techniques developed for two-level circuits can now be applied, with several modifications to the ENF's.

H. Boolean Difference Method

The Boolean difference is not new. A paper by Akers [1] described it several years ago as a mathematical tool. The idea of using the Boolean difference for error analysis was suggested to L. W. Bearnson by Prof.E. Stabler, Syracuse University, in 1965 [5]. A paper describing similar ideas was published in 1967 [3]. It seems that the originator of difference methods was G. Boole, even though he did not apply them to Boolean equations [7].

The need for a conceptually simple and straightforward ways of deriving test sequences for combinational circuits is the impetus behind the Boolean difference methods. Boolean difference is defined as being the exclusive-or operation between two boolean functions, one representing the normal circuit and other representing the faulty circuit. Thus if the Boolean difference is a 1, a fault is indicated. Assume that there is a switching function that has one output F and n inputs $x_1,x_2,\ldots.x_n$, so $F(X) = F(x_1,x_2,\ldots.,x_n)$. If one of the inputs to the switching function was in error, say input x_i , then the output would be $F(x_1,\ldots..,x'_i,\ldots\ldots,x_n)$.To analyze the action of the circuit when an error occurs, it is desirable to know under what circumstances the two outputs are the same[5].

I. SPOOF Method

An efficient and easy-to-drive method for obtaining tests for detection of single and multiple faults is presented which is based on the use of the *Structure and Parity Observing Output Function* (SPOOF). SPOOF provides the information needed for complete analysis of the effects of possible faults on the functional characteristics of a given circuit.

The structure- and parity-observing output function (SPOOF) with the adjective disjunctive indicates that repeatedly used the distributive property u(v V w) = uv V uw to obtain an expression in disjunctive normal form (i.e., "sum-of-products" form). By using instead, the distributive property u V vw = (u V v)(u V w), one can obtain a similar expression for the network output function in "product-of-sums" form called a conjunctive SPOOF.

SPOOF have introduced, also exhibits similarities to the output functions expressed in terms of "literal propositions" as developed by Poage [12]. It will be apparent, however, that the SPOOF provides a much more compact and

somewhat more tractable and more easily derived notation for the information needed for complete analysis of the effects of possible faults on the functional characteristics of a given network. Each term of the disjunctive SPOOF looks very similar to a conjunction of the elements of a P set, as the latter are defined by McCluskey [11]. Before we formally define SPOOF's, in fact, some useful extensions of the concepts of P sets and S sets. The application of the SPOOF to the analysis of the effect of any single and multiple s-a-0 and s-a-1 on the output function of a circuit is based on the this method.

J. Genetic Algorithm Method

The two methods Fixed Scheduled Fault Detection and Heuristic test minimization adapted for test minimization requires very large fault table to be constructed. Genetic Algorithm approach proposed in this work overcomes the problem of creating a very large fault table. Test numbers are chosen at random and evolutionary strategy is used for improving the solution. Binary combinations of only chosen tests in a genome(chromosome) are generated and their fitness are evaluated[18]. The entire fault table need not to be constructed. Fault table construction is based on random numbers generated in each generation. Genetic Algorithm consumes less memory location for minimization process. The best-fit solutions in one stage are carried over to another stage and worst-fit solutions are eliminated[19]. Genetic Algorithms greatly lies on random numbers generated. Optimal solution is not guaranteed in all cases. It necessitates repetition of the process with fresh random numbers, when optimal solution is reached. Hence the execution time will not be stable in all cases.

K. Integer Linear Programming Method

In Integer Linear Programming Method[ILP], two tables are generated for the given combinational circuit(boolean expression in sum-of-products form). They are fault table(Table 1) and fault detection table(Table 2). Based on fault detection table fault diagnostic matrix is formed[20]. The diagnostic matrix Fjn is formed with test number rows and zf_1, zf_2 ..zf_i columns alone as shown in Table III.

TABLE III. DIAGNOSTIC MATRIX $\{F_{JN}\}$.

Test number (J)	**Fault number (n)**							
	1	2	3	4	. . .	. . .	n
1	1	0	0	0	. . .	. . .	0
2	1	0	1	0	. . .	. . .	1
3	0	1	0	1	. . .	. . .	0
.	.	.	.	.	. . .	. . .	.
.	.	.	.	.	. . .	. . .	.
J	0	0	1	0	. . .	. . .	1

In the above matrix rows identifies test numbers and columns identifies fault numbers. The Primal ILP is formulated from fault diagnostic matrix.

Suppose a combinational circuit has n faults, integer values {0,1} are assigned to variables f_1, f_2, …, f_n. in the fault set F. Vector set V with n inputs for each test number j is assigned integer values {0, 1} for variables V_j, j = 1, 2, . . . , J (where J is 2^n), to each vector. Without loss of generality, it is assumed that all n faults are detected by these vectors[8]. The problem of finding the minimal test set is to find the smallest subset of these vectors that detects all the faults. In this primal problem, the test set is chosen as follows: The vector j is included in the selected vector set, if $V_j = 1$. The vector j is discarded in the selected vector set, if $V_j = 0$.

The fault set and test set are simulated without dropping faults. The result is represented as a diagnostic matrix of 0's and 1's as shown in Table III. In this matrix, an element $F_{jn} = 1$ only if fault n is detected by vector j. The ILP problem is stated as,

$$\text{Minimize} \quad \sum_{j=1}^{J} V_j \tag{2}$$

$$\text{Subject to:} \quad \sum_{j=1}^{J} F_{jn} V_j \geq 1, \quad n = 1, 2, \ldots, n \tag{3}$$

$$v_j \in \text{integer } \{0, 1\}, \quad j = 1, 2, \ldots, J \tag{4}$$

This problem minimize the number test cases covered by maximum number of faults present in the circuit. This method can be adopted for complex VLSI circuits and results best optimal solution with exponential complexity.

V. COMPARISON OF THE ABOVE DISCUSSED METHODS

In Table IV, advantages and limitations of fault detection and test minimization methods discussed in section IV are tabulated.

TABLE IV. COMPARISION TABLE

Sl No	**Methods**	**Advantages**	**Limitations**
1	Fault Table Method	Suitable for Simple circuits	It requires the construction of fault table
2	Heuristic Method	Suitable for Simple and tree-like circuits	It requires the construction of fault table and extensive computations for isolating fault-free from faulty responses.

3	Path Sensitizing Method	Suitable for Non-tree like circuits. The path-sensitizing method is very attractive from the point of view of not requiring the construction of the fault table.	The process of exploring all the possible paths originating from the output of gates involves a lot of searching operations.
4	Equivalent-Normal-Form Method	ENF method detects certain paths that are not sensitizable in other methods.	The method does not guarantee a complete diagnosis of the given circuit as the scoring technique employed yields a completely different paths for ENF and its complement.
5	Two- Level-Circuit Fault Detection Methods: Karnaugh Map Method and Tabular Method	A very simple and direct methods suitable for any two-level AND-OR(OR-AND,NAND-OR,etc) irredundant circuits. Tabular method does not employ k-map technique.	The Karnaugh map method requires irredundant circuits with a maximum of 6 input variables only. Although Tabular method does not restrict the number of variables, irredundancy is a constraint.
6	Multilevel-circuit Fault Detection	This can be applied to multilevel circuits with more than two levels.	Irredundancy is a constraint.
7	ENF-Karnaugh map Method	It is much simpler technique than the ENF method, as it does not use a scoring technique and is without the complemented ENF.	Restricted to two level AND-OR circuits only.
8	Boolean Difference Method	Conceptually simple and straightforward ways of deriving test sequences for combinational circuits.	Suitable for Simple digital circuits only. Complexity of computation increases with the number of inputs.
9	SPOOF Method	An efficient and easy-to-drive method for the detection of single and multiple faults.	Suitable for Simple digital circuits only.
10	Genetic Algorithm Method	Adopts evolutionary techniques to arrive at compact test set. It eliminates the need for a very large fault table and thereby reduces the space complexity to a greater extent. The method is suitable for any complex circuits.	Genetic Algorithms greatly rely on random numbers. Optimal solution is not guaranteed always.
11	Integer Linear Programming Method	It can be adopted for complex VLSI circuits. Optimal solution is assured.	Space complexity is exponential.

VI. CONCLUSION

In this paper, the authors surveyed the methods for fault detection and test minimization in two stage combinational circuits. Totally 11 methods that range from very basic methods to the recent fast evolutionary(genetic) methods are studied. Merits and demerits of those methods are presented. Iterative methods yield optimal solutions for circuits of various complexity. Genetic methods, as they greatly rely on random numbers, yield near optimal solutions with the advantage of lesser space and time complexity compared to iterative methods. The next phase of the research is in progress to devise a new method for minimizing test set in VLSI combinational circuits with ILP and evolutionary concepts.

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