International Journal of Computer Trends and Technology- volume3Issue3- 2012

Implementation of SOBEL Edge Detection on FPGA

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***Abstract*—The image processing algorithms has been limited to software implementation which is slower due to the limited processor speed. So a dedicated processor for edge detection is required which was not possible until advancements in VLSI technology. The proposed work presents FPGA based architecture for Edge Detection using Sobel operator. Sobel operator is chosen due to its property of less deterioration in high levels of noise.**

The problem of the present dissertation can be stated simply and as follows

1. **Study of edge detection**
2. **To implement Sobel Edge detection on FPGA**

Keywords- Edge detection, Sobel operator, FPGA

I. INTRODUCTION

Field Programmable Gate Array (FPGA) technology has become an alternative for the implementation of software algorithms. The unique structure of the FPGA has allowed the technology to be used in many applications from video surveillance to medical imaging applications. FPGA is a large-scale integrated circuit that can be re-programmed. The term "field programmable" refers to ability of changing the operation of the device. Gate array refers to the basic internal architecture that makes re-programming possible. Implementations of real-time image processing algorithms can be done on general purpose microprocessors. The application of FPGA in image processing has a large impact on image or video processing. This is due to the potential of the FPGA to have parallel and high computational density as compared to a general purpose microprocessor. This step is coupled together with the ability of FPGA of being re-programmable that adds flexibility in the development of image processing algorithms on FPGA. During the recent years FPGAs have become the dominant form of programmable logic.

A.Edge detection

Edge detection is a method of determining the discontinuities in gray level images. Edges are one of the most important elements in image analysis and processing in computer vision because they play quite a significant role in many applications of image processing particular for machine vision. However no edge detection algorithm can successfully discover edges for diverse images and no specific quantitative measure of the quality for edge detection is given at present.
Conventional edge detection
Mechanisms examine image pixels for abrupt changes by comparing pixels with their neighbours. This is often done by detecting the maximal value of gradient such as Roberts, Prewitt, Sobel, Canny and so on all of which are classical edge detectors.

II. IMPLEMENTATION OF IMAGE EDGE DETECTION USING FPGA

The edges of image are considered to be most important image attributes that provide valuable information for human image perception [1,3]. The edge detection is a terminology in image processing particularly in the areas of feature extraction to refer to algorithms which aim at identifying points in a digital image at which the image brightness changes sharply [4,5]. The data of edge detection is very large so the speed of image processing is a difficult problem. FPGA can

overcome it [6]. Sobel operator is commonly used in edge detection. Sobel operator has been researched for parallelism [7] but Sobel operator locating complex edges are not accurate. It has been researched for the Sobel enhancement operator in order to locate the edge more accurate and less sensitive to noise but the software cannot meet the real-time requirements [8].

A.Sobel Edge Detection Enhancement Algorithm

The Sobel operator is a classic first order edge detection operator computing an approximation of the gradient of the image intensity function. At each point in the image the result of the Sobel operator is the corresponding norm of this gradient vector. The Sobel operator only considers the two orientations which are 0 and 90 degrees convolution kernels as shown in Fig. 1.

-1	0	1
-2	0	2
-1	0	1
Gx		

-1	-2	-1
0	0	0
1	2	1
Gy		

Figure 1. Convolution Kernels in X and Y direction

These kernels can then be combined together to find the absolute magnitude of the gradient at each point. The gradient magnitude is given by:

$$|G| = \sqrt{G_x^{\,2} + G_y^{\,2}}$$

Typically an approximate magnitude is computed using:

$$|G| = |G_x| + |G_y|$$

This is much faster to compute.

The sobel operator has the advantage of simplicity in calculation. But the accuracy is relatively low because it only used two convolution kernels to detect the edge of image.

B.FPGA Hardware Implementation

This design uses 3×3 convolution kernels processing 640×480 Gray Scale Image from the database in personal computer. The architecture is shown in Fig. 2. The system is divided into four modules: 3× 3 pixel generation module, Sobel enhancement operator module, edges control module and binary segmentation [9,10]. In this system, Clk is the clock signal, Data input is the pixel signal of Gray Scale Image, Result is the result of edge detection operator signal, Generation data and Data are the middle signal [2]. The function and structure of each module are as follows:

The structure of 3×3 pixel generation module is shown in Fig. 3. This module consists of 3 shift register groups and two FIFO. The FIFO is used to cache a line of image data. The image data is input according to the clock signal so P1, P2, …., P9 is the 3×3 image data template. When the data is continuously input, 3×3 image data template changes. It can contain all pixels of an image. The FIFO is generated by dual-port RAM [11] .

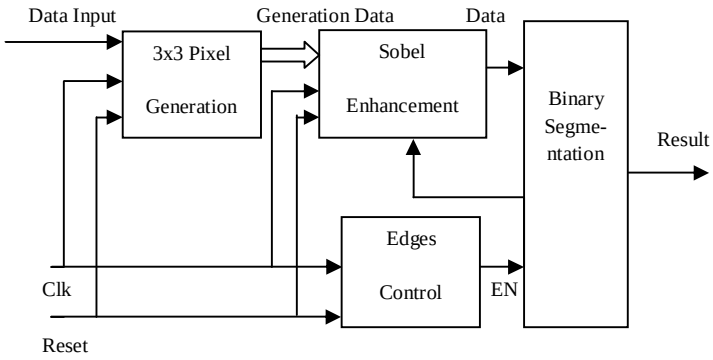
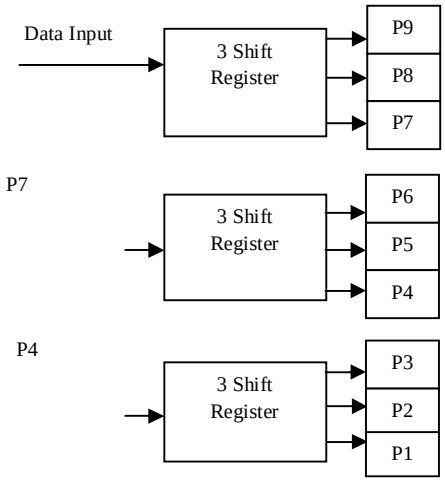


Figure 2. Architecture

In Sobel enhancement operator module the orientation convolution kernel uses parallel processing construction. The orientation convolution result is compared with each other and then the maximum value is the output. The pipeline structure is used to calculate each orientation convolution kernel. It is six corresponding input data because three coefficients of each convolution kernel are zero multiplied by 2. The structure is shown in Fig.4.



s

Figure 3. 3x3 Pixel Generation Module

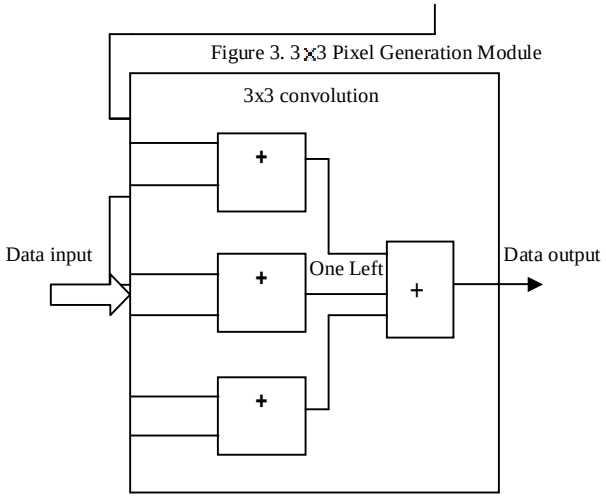


Figure 4. Convolution Structure

The structure of edges control module is shown in Fig. 5. Clk is the clock signal and Reset is the reset signal. Turn is enable signal when the Turn is valid the module works. EN is the output data control signal. This module can know where the current pixel location is and whether it is the edges of the image. Sobel edge detection enhancement operator can not deal with the left edge, right edge, the up edge and down edge. In this design the result of the edge pixels is set to zero otherwise call the Sobel enhancement operator module.

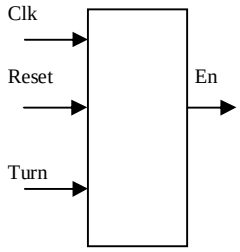


Figure 5. Edges Control Module

The structure of binary segmentation module is shown in Fig. 6. EN is the output data control signal. Data is the result of the Sobel enhancement operator module. Result is 0 or 255. In this module the final result is the binary image of edge detection having only two pixel values according to the given threshold value i.e. 0 and 255.

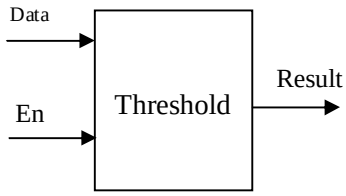


Figure 6. Binary Segmentation

III. EXPERIMENTAL RESULTS

The experimental results for image edge detection in Verilog are shown below:

Fig. 7(a) is the original image for Edge Detection.

Fig. 7(b) shows gray scale image for Edge Detection.

Fig. 7(c) shows edge detection result using Verilog.

Figure 7(a)

Figure 7(b)

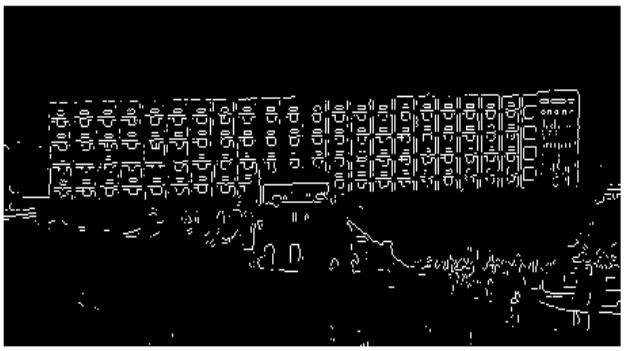


Figure 7(c)

IV. CONCLUSION

The hardware was realized on a Altera FPGA kit. The processor was coded using Verilog and simulated using Modelsim 6.5e. The execution time for the entire program of edge detection for an image of size 640× 480 is few seconds.

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