High performance Level Conversion Flip Flop for Dual Supply Systems

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Abstract **– In this paper high performance level conversion flip flop has been designed. The circuit has been designed by reducing internal switching activity and glitches. The new FF has introduced with conditional discharged to reduce the power consumption. This Conditional Discharge Flip Flop (CDFF) not only reduces the internal switching activities, but also generates less glitches at the output, while maintaining by maintaining minimum delay between D-to-Q. The proposed flip-flop can save up to 19% of the energy with the same speed as that of conventional level converter with bit area overhead.**

Index Terms: **Dual supply, level conversion, low power, conditional discharge.**

I. INTRODUCTION

The clock system, composed of the clock interconnection network and timing elements (flip-flops and latches), is one of the most power consuming components in a very large scale integration (VLSI) system. It accounts for 30%–60% of the total power dissipation in a system. Moreover, in order to sustain the trend of higher performance and throughput, more timing elements will be employed for extensive pipelining of not only data path sections, but also global bus interconnects, causing the power dissipation of the clock system to become more dominant[1],[10]. As a result, reducing the power consumed by flip-flops will have a deep impact on the total power consumed. In addition, from a timing perspective, flip-flop latency consumes a large portion of the cycle time while the operating frequency increases. Accordingly, flip-flop choice and design has a profound effect both in reducing the power dissipation and in providing more slack time for easier time budgeting in high-performance systems. This output driver arrangement requires complementary drive signals for the two NMOS transistors, which can be accomplished by simply adding an inverter. However, if the raw input and its complement were used to drive the NMOS transistors directly there would be a significant short circuit current during switching. When the input rises there is a brief period of time, equal to the delay through the inverter, when the input signal and its complement signal are both high. If these two signals drove the NMOS transistors directly then both transistors would be enabled at the same time, providing a low impedance path from *VDD* to ground. The resulting current spikes would introduce considerable noise into the power supply rails and would increase the chip's power consumption. Using double-edge triggering, where data latching or sampling is issued at both the rising and falling edges, usually allows the clock routing network to consume less power [4],[5]. For example, for a system with a throughput of one operation per cycle and a clock frequency f, double-edge triggering results in two operations being executed in one cycle; if we use half the frequency, we can maintain the same throughput of the original system.

One effective technique to obtain power savings inside a flip-flop can be devised by realizing the fact that a common property among various high-speed flip-flops is the utilization of dynamic structure. This dynamic behaviour causes a lot of power to be wasted as a result of unnecessary internal switching activity, especially in moderate or lower data activity environments. Reducing these activities can effectively result in reducing the overall power dissipation[15],[16].In this regard, several existing approaches to reduce the internal switching activity are surveyed and classified into conditional recharge and conditional capture techniques. This paper reviews these techniques with some associated flip-flops utilizing these techniques. Also, a new technique, Conditional Discharge[3],[5],[9], is proposed in this paper. This new technique not only reduces the internal switching activity of flip-flops but also overcomes the limitations associated with some of the techniques mentioned above.

II. EXTING LEVEL CONVERSION FLIP FLOP

The differential level-shifting scheme normally has large delay and power overhead due to crossover contention and SLLS has larger delay and power consumption than PHL. CSSA consumes dynamic power in addition to the crossover contention problem.

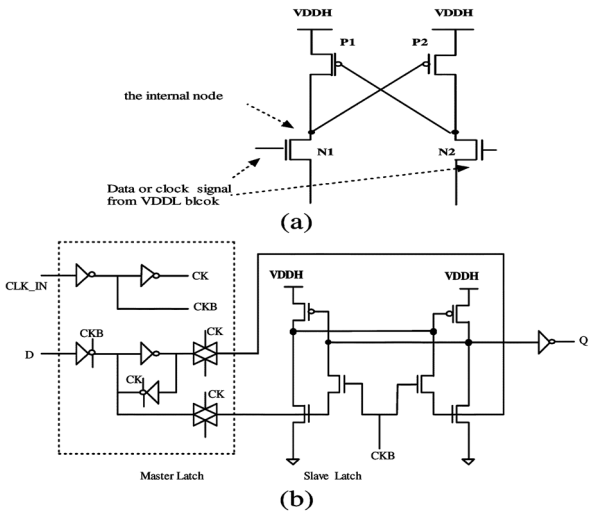

Fig 1(a) & (b) Existing level converters

MSHL has larger PDP than PHL due to the long critical path (five gates) resulting in large delay, and it dissipates more power than PHL. PPR dissipates more energy than PHL, thus losing its advantage in CVS systems[6],[13]. SPFF has an overhead of the last two inverters in the critical path, as well as eight more transistors than PHL (a 33% increase in the number of total transistors), and it consumes more power than PHL as shown in fig.1(a) and (b). PHL is the most efficient design in view of power consumption among LCFFs including SLLS, CSA, MSHL, PPR, and SPFF. We will not discuss SLLS, CSA, MSHL, PPR, and SPFF further in this paper due to their relatively higher power consumption than PHL[14]. Balanced reduction of both power and delay of an LCFF is the main method to reach improved power savings in a CVS system [6]. PHL is the best example of this in comparison with other previous designs such as PPR. However, PHL has a threshold drop problem aggravated by the low voltage of the input, and it has an explicit pulse generator, which normally consumes more power. Furthermore, it has four gates on the critical path. NMOS branch is responsible for pulling the voltage down. The clocked pseudo NMOS scheme is different from other conventional pseudo NMOS logics. we use clocked transistors in the pull-down branch as well as a conditional discharge feedback to control transistor. Comparing this with previous published level-shifting schemes[10], the proposed level-shifting scheme employs only one single PMOS, resulting in an efficient design. One thing to note is that pulsed flip-flops might need more hold time than conventional flip-flops[3].

III. PROPOSED LEVEL CONVERSION FLIP FLOP

The schematic diagram of the proposed flip-flop, conditional discharge flip-flop (CDFF), is shown in Fig. 2. The flip-flop is made up of two stages. Stage one is responsible for capturing the LOW-to-HIGH transition. If the input is HIGH in the sampling window, the internal node is discharged, assuming that were initially (LOW, HIGH) for the discharge path to be enabled. As a result, the output node will be charged to HIGH through P2 in the second stage. Stage 2 captures the HIGH-to-LOW input transition. If the input was LOW during the sampling period, then the first stage is disabled, and node retains its pre charge state. Whereas, node will be HIGH, and the discharge path in the second stage will be enabled in the sampling period, allowing the output node to discharge and to correctly capture the input data. The conditional discharging scheme is employed in the CDFF as follows: in order to reduce the redundant switch power, we employ a discharge control transistor N5 at the discharge path of the first stage. When, which means and, N5 turns on, and the discharge path is enabled. If the input makes a LOW-to-HIGH transition, and CLK pulse is HIGH, N1, N5, and N3 switch on, the internal node is discharged to LOW, and is pulled up to HIGH with pulled down to LOW, which shuts off the nMOS stack in first stage. For this transition (LOW-to-HIGH), is discharged only once; i.e., consecutive HIGH level at will not be sampled because the discharging path is inhibited.

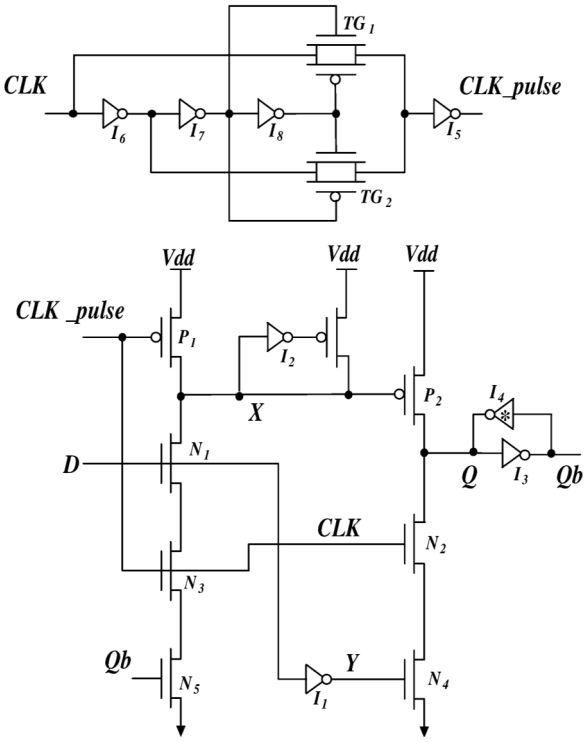

Figure 2: Proposed level converter

To ensure that the HIGH-to-LOW transition is sampled by the flip-flop, dual path is used. Recall that the output rise transition tends to be the slow path (critical path); by employing dual path, capacity at node is reduced, and thus the LOW-to-HIGH delay could be reduced. Setup used for the flip-flops simulations. Inputs are driven by inverters, and the output is driving a load of 14 minimum inverters (FO14).issue in mixed signal circuits. Moreover, node stays HIGH or pre charged in most cases, which helps in simplifying the keeper structure as shown in Fig. 2, and it also reduces the capacitive load at node. Double-edge triggered pulse generator is utilized to further reduce power on the clock tree and the clocked transistors in pulse generator. Double-edge triggered flip-flops can have the same data throughput as the single-edge triggered flip-flops. The power saved in the clock distribution network is not included. When we compare the power consumption. Also, clock gating can be easily applied to eliminate power consumption when keeps the same value. Although the input load is increased, the overall power saving could be achieved significantly.

IV.SIMULATION RESULTS

The simulation results of flip-flops were obtained in a 90nm CMOS technology at room temperature using

HSPICE, the supply voltage is 1.2 V as shown in the figure 3 and 4. In order to obtain accurate results, we have simulated the circuits in a real environment, which dictates that the flip-flops' inputs (clock, data) are driven by fixed input buffers, and the outputs are required to drive an output load. The value of the capacitance load at output node is selected to simulate a fan out of fourteen standard sized inverters (FO14) for the technology in use. Assuming uniform data distribution, we have supplied the input with 16-cycle pseudorandom input data with activity 19% to reflect the average power consumption. The input pattern "1010" represents maximum input switching act "1111" and "0000" represent zero switching activity. A clock frequency of 250 MHz is used for single-edge triggered flip-flops, whereas a 125-MHz frequency is used for double-edge triggered flip-flops. Power consumed in data and clock drivers are included in our measurements. Circuits were optimized for minimum power delay product, PDP. The D -to- Q delay is obtained by sweeping the LOW-to-HIGH(1-1.2)V and HIGH-to-LOW(1.2-1)V data transition times with respect to the clock edge, and the minimum data to output delay corresponding to optimum setup time is recorded. Minimum D -to- Q delay is an appropriate metrics for flip-flops.

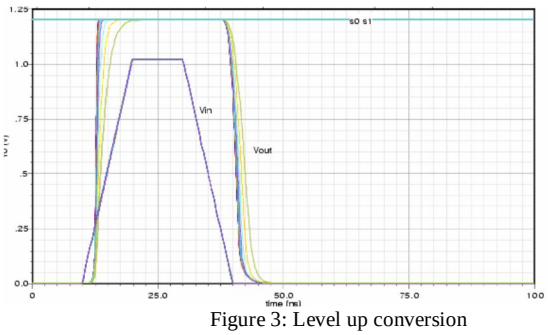

Figure 3: Level up conversion

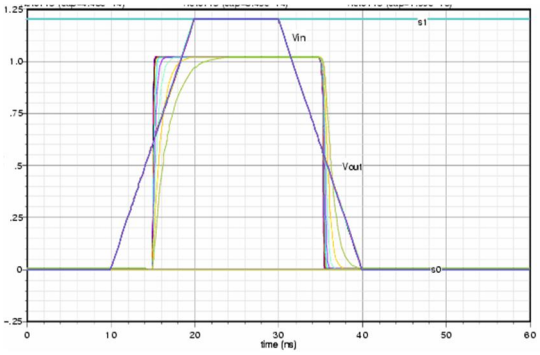

Figure 4: Level down conversion

V. CONCLUSION

The design is carried out for its power and load analysis. These two analyses prove that the proposed level converter design is not only a low power design but it also provides a stable output under varying load conditions. The power analysis proved that the design of level converter produces a very stable output at low voltage as well as high voltage at 90nm design. The power analysis results prove that the level converter has a power dissipation reduction of about 19 % as compared to other level converter designs at a different technology.

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