Adiabatic Logic For Low Power Application Using Design 180nm Technology

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ABSTRACT: Adiabatic circuits and standard CMOS logic are widely employed in Low power VLSI chips to achieve high system performance. The power saving of adiabatic circuit can reach more than 90% compared to conventional static CMOS logic. The clocking schemes and signal waveforms of adiabatic are different from those of standard CMOS circuits. This thesis work demonstrates the low power dissipation of Adiabatic Logic by presenting the results of designing various design/ cell units employing Adiabatic Logic circuit techniques(an inverter, a two-input NAND gate, a two-input NOR gate, a two-input XOR gate, a two-to-one multiplexer and a one-bit carry Adder) This paper also investigates the different power delay product over the wide range of supply voltages. Power dissipation has been calculated for different values.

Keywords: Low Power, Adiabatic logic, Energy dissipation, Positive Feedback Adiabatic Logic, Energy recovery

I NTRODUCTION

Demands for low power and low noise digital circuits have motivated VLSI designers to explore new approaches to the design of VLSI circuits. Energy recovering (adiabatic) logic is a new promising approach, which has been originally developed for low power digital circuits [1-3]. Adiabatic circuits achieve low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their capacitors . Another major advantage of adiabatic logic families is their best behavior for lower generation of switching noise, which is becoming one of the most important problems in current digital and especially in mixed mode integrated circuits. The traditional solution of employing on chip decoupling capacitors to combat the supply noise results in an unacceptable area increase . Invoking adiabatic logic circuits will reduce the switching noise of digital circuits. The reason is that in these circuits, the switching occurs with the minimum voltage drop across devices and nodes voltages change slowly[9]. To the best of our knowledge no report on the efficiency of the switching noise characteristic of the adiabatic logic circuits has been published in the literature. In this paper, we present the comparison and simulate Positive Feedback Adiabatic Logic (PFAL) based on INVERTER, NAND, NOR, XOR and 2:1 MUX, ONE-BIT CARRY ADDER

Operation Of Adiabatic Logic

The word *ADIABATIC* comes from a Greek word that is used to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In real-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, one can achieve very low energy dissipation by slowing down the speed of operation and only switching transistors under certain conditions[4]. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as *ENERGY RECOVERY CMOS***.**

In the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems

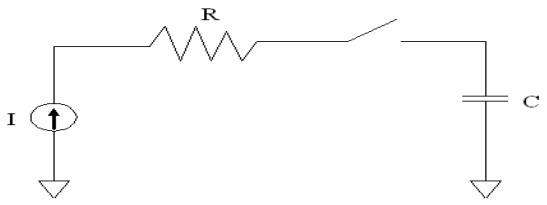


Fig1. Circuit for Adiabatic Switching.

Here, the load capacitance is charged by a constant-current source (instead of the constant-voltage source as in the conventional CMOS circuits). Here, R is the resistance of the PMOS network. A constant charging current corresponds to a linear voltage ramp[9]. Assume, the capacitor voltage V_C is zero initially.

The voltage across the switch = IR

$P(t)$ in the switch =I^2R (1)

Energy during charge = $(I^2R)T$

$$E=(I^2R)T=(CV/T)^2\,RT=C^2V^2/T\,R \qquad (2)$$

$$E = E_{dis}=(RC/T)CV^2=(2RC/T)\,(1/2CV^2) \qquad (3)$$

where, the various terms of Equation (3) are described as follows:

E — energy dissipated during charging,
Q — charge being transferred to the load,
C — value of the load capacitance,
R — resistance of the MOS switch turned on,
V — final value of the voltage at the load,
T — time spent for charging.

Now, a number of observations can be made based on Equation (3) as follows:

(i) The dissipated energy is smaller than for the conventional case, if the charging time *T* is larger than *2RC*. That is, the dissipated energy can be made arbitrarily small by increasing the charging time,

(ii) Also, the dissipated energy is proportional to *R*, as opposed to the conventional case, where the dissipation depends on the capacitance and the voltage swing. Thus, reducing the on-resistance of the PMOS network will reduce the energy dissipation

Adiabatic Logic Families.

Practical adiabatic families can be classified as either Partially adiabatic or fully adiabatic. In partially adiabatic circuit, some charge is allowed to be transferred to the ground, while in fully adiabatic circuit all the charge on the load capacitance is recovered by the power supply[9]. Fully adiabatic circuits face so many problems with respect to operating speed and input power clock synchronization. Different logic families are Efficient Charge Recovery Logic (ECRL)[9], 2N- 2N2P Adiabatic Logic,Positive Feedback Adiabatic Logic (PFAL),NMOS Energy Recovery Logic (NERL), Clocked Adiabatic Logic (CAL),True Single-Phase Adiabatic Logic (TSEL),Source-coupled Adiabatic Logic (SCAL),Two phase adiabatic static CMOS logic(2PASCL) and fully adiabatic logic families are ,Pass Transistor Adiabatic Logic (PAL),Split- Rail Charge Recovery Logic (SCRL). In this project we are going with Positive Feedback Adiabatic Logic (PFAL)[6],

II POSITIVE FEEDBACK ADIABATIC LOGIC

Positive feedback adiabatic logic was introduced in 1996 by Vetali and shows very positive aspects in addressing the power issues[6]. The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) has been used, since it shows the lowest energy consumption if compared to other similar families, and a good robustness against technological parameter variations. It is a dual-rail circuit with partial energy recovery. The general schematic of the PFAL gate is shown in Figure 2 The core of all the PFAL gates is an adiabatic amplifier, a latch made by the two PMOS *M1-M2* and two NMOS *M3-M4*, that avoids a logic level degradation on the output nodes *out* and */out*. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The functional blocks are in parallel with the PMOSFETs of the adiabatic amplifier and form a transmission gate. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs[6].

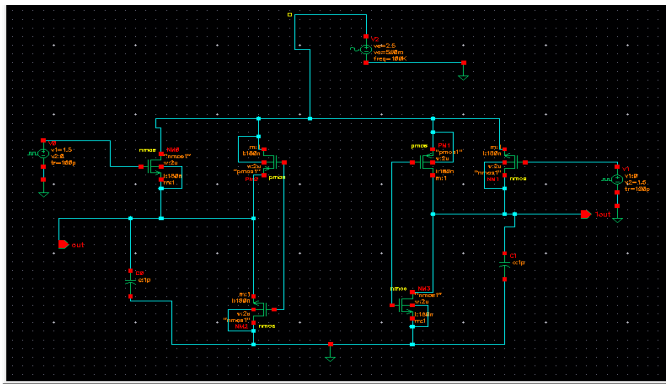


Fig 2. Positive feedback adiabatic logic.

III DESIGN AND SIMULATION FOR AN ADIABATIC

A PFAL two-input NAND/ AND.

The partially adiabatic PFAL two-input NAND/ AND gate can be implemented as shown below in the Figure 3 using CADENCE and simulated waveforms is shown in Figure 4. Power dissipation against operating frequency is shown in figure

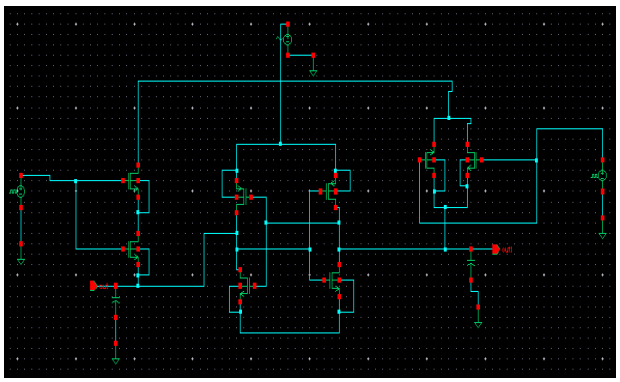


Fig3. adiabatic PFAL two-input NAND/ AND.

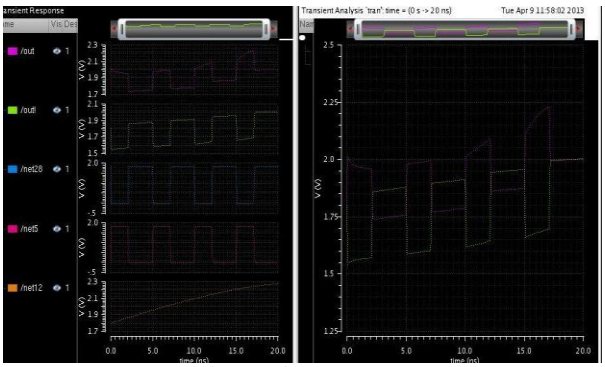
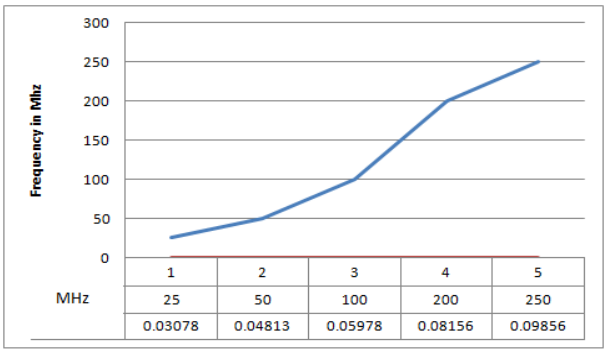


Fig4 simulated waveforms of two-input NAND/ AND.



MHz	1	2	3	4	5
	25	50	100	200	250
	0.03078	0.04813	0.05978	0.08156	0.09856

Fig5. Power dissipation(µW) against operating frequency.(MHz)

DESIGN AND SIMULATION FOR AN ADIABATIC PFAL TWO-INPUT OR / NOR GATE

An adiabatic PFAL exclusive-OR gate is implemented as below in Figure 6 and simulated waveforms are as shown in Figure 7 respectively. The minimum-sized XOR gate implemented will show lesser power dissipation as compared to the conventional CMOS logic.

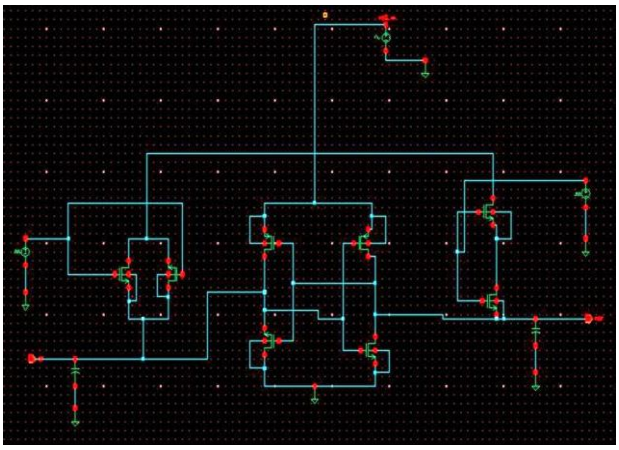


Fig6. PFAL two-input OR/NOR gate.

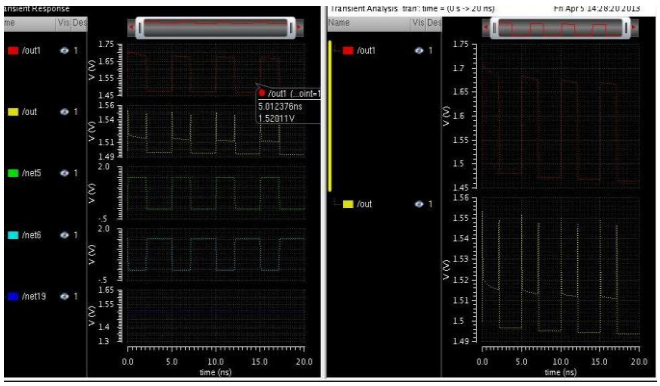
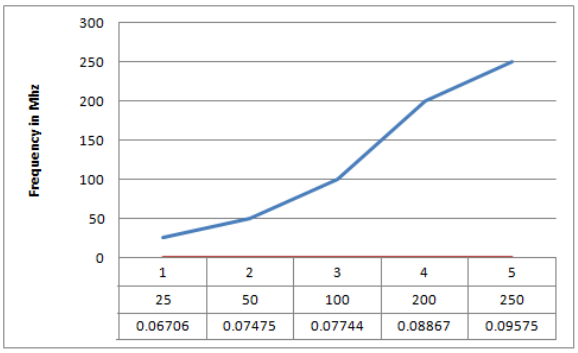


Fig7 simulated waveforms PFAL two-input OR/NOR gate.



	1	2	3	4	5
	25	50	100	200	250
	0.06706	0.07475	0.07744	0.08867	0.09575

Fig8 Power dissipation(µW) against operating frequency(MHz)

DESIGN AND SIMULATION FOR AN ADIABATIC PFAL TWO-INPUT XOR / XNOR GATE

An adiabatic PFAL exclusive-OR gate is implemented as below in Figure 9 and simulated waveforms are as shown in Figure 10, respectively. The minimum-sized XOR gate implemented will show lesser power dissipation as compared to the conventional CMOS logic

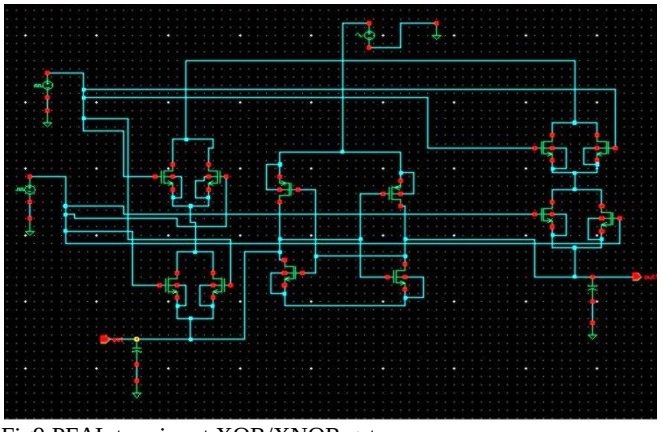


Fig9 PFAL two-input XOR/XNOR gate.

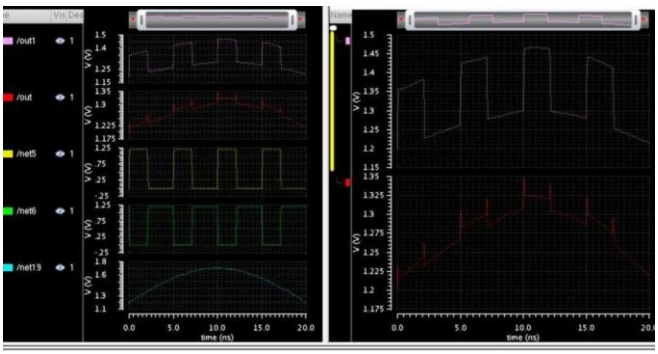
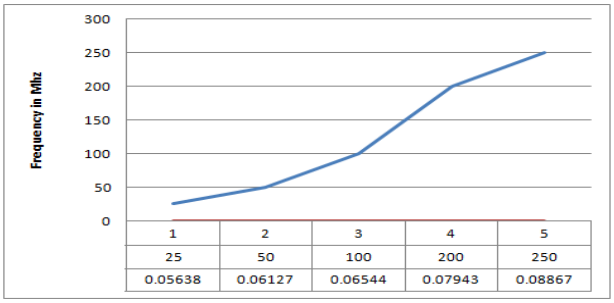


Fig10 simulated waveforms PFAL two-input XOR/XNOR gate.



1	2	3	4	5
25	50	100	200	250
0.05638	0.06127	0.06544	0.07943	0.08867

Fig11 Power dissipation(μW) against operating frequency(MHz)

DESIGN AND SIMULATION FOR AN ADIABATIC PFAL 2:1 MULTIPLEXER

An adiabatic PFAL two-to-one Multiplexer can be implemented in CADENCE It implements the function *F* = (*A*) (*/S*) + (*B*) (*S*) as illustrated in the Figure 12, respectively. When the select (*S*) signal is low, it outputs the signal *A* and when the select (*S*) signal is high, it outputs the signal *B*, respectively and its functionality can be proven with the help of simulated waveforms as shown in the Figure 13.

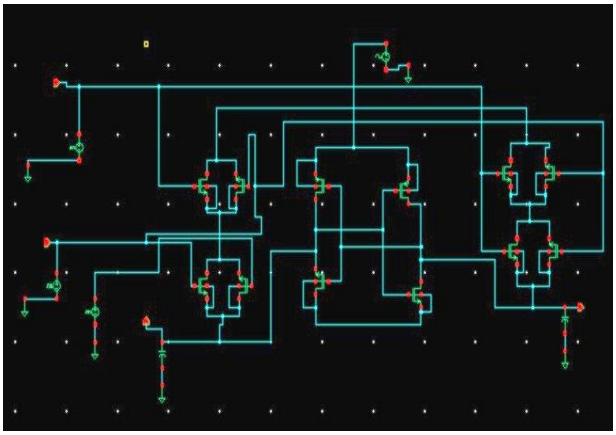


Fig12 PFAL 2:1 MUX.

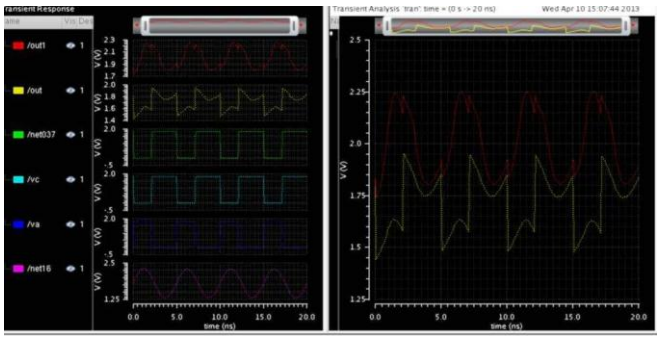
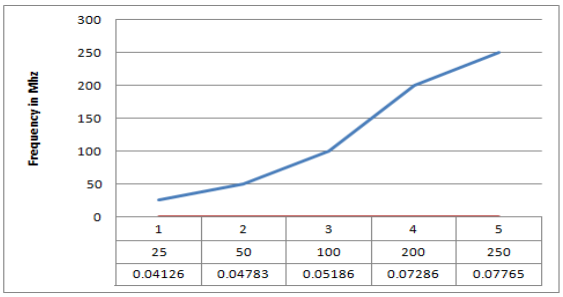


Fig13 simulated waveforms PFAL 2:1 MUX.



1	2	3	4	5
25	50	100	200	250
0.04126	0.04783	0.05186	0.07286	0.07765

Fig14 Power dissipation(μW) against operating frequency(MHz)

DESIGN AND SIMULATION FOR AN ADIABATIC PFAL ONE-BIT CARRY ADDER

An adiabatic PFAL CARRY adder gate is implemented as below in Figure 15 and simulated waveforms are as shown in Figure 16 respectively. The minimum-sized carry gate implemented will show lesser power dissipation as compared to the conventional CMOS logic

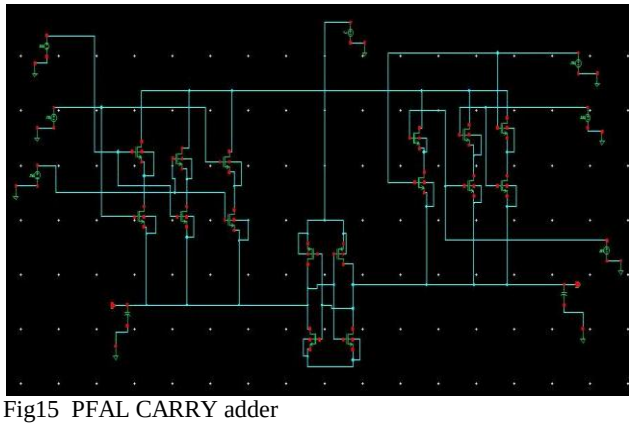


Fig15 PFAL CARRY adder

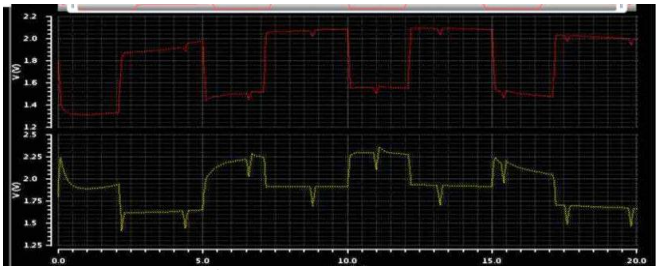


Fig16 simulated waveforms PFAL CARRY adder.

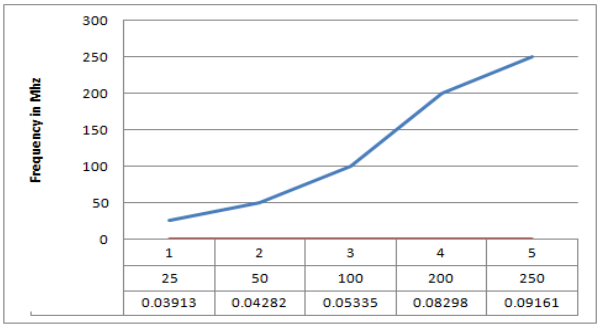


Fig17 Power dissipation(μW) against operating frequency(MHz)

power dissipation comparison at different output load capacitances which have been plotted for different logic gates operating frequency(25).

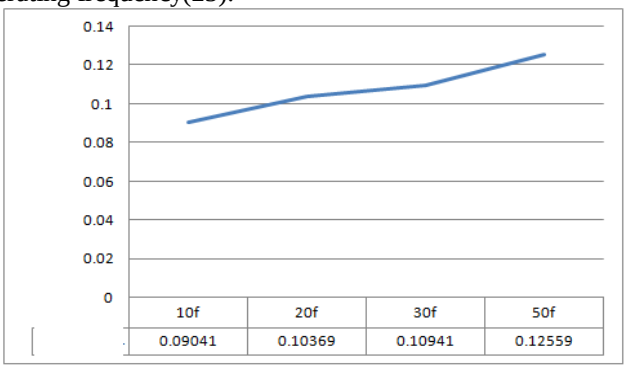


Fig18 Power dissipation(μW) against different output load capacitances(fF).

IV CONCLUSION

We present a low power adiabatic circuit based on PFAL circuit. It was found that the adiabatic PFAL logic style is advantageous in applications where power reduction is of prime importance as in high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants. With the adiabatic switching approach can be used to reduce the power dissipation of the digital system with the help of adiabatic logic the energy saving of upto76%to90% can be reached.

After the study the adiabatic we realize that improving adder is very difficult because of transistor level. If we want to get higher performance we must reduce the complexity in transistor level. Adiabatic circuit are slow by today's standards. Requires 50% more area than static CMOS.(more transistor is required).

ACKNOWLEDGMENT

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