Implementation of Flash ADC using Multisim Technology

Raghavendra.R[1], Dr S.A Hariprasad[2]

[1]Instructor, [2]Professor Department of Electronics and Communication Engineering
RV College of Engineering Bangalore -560 079.

Abstract **– Resolution, Speed, and Power consumption are the three key parameters for an Analog-to-Digital Converter (ADC) and Flash ADCs are the fastest type of ADC. In this paper an effort is made to design 3-bit and 8-bit Flash ADC using multisim. Flash ADC very useful for high-speed applications such as radar detection, wide band radio receivers and communication links. More often the flash ADC is embedded in a large IC containing many digital decoding functions. The integrated flash ADC is operated at 3 and 8-bit precision with analog input voltage of -10.0Vdc to +10.0Vdc. The ADC has been designed, implemented & analysed using Multisim tool and this paper provides a detailed view of a 3 bit and an 8 bit Flash ADC using comparators, 7segment display (Hex value) and actual working explanation about Flash ADC with step by step accurate simulated output using Multisim. The simulated output shows higher range of accuracy (seven digits) is obtained when Flash ADC is experimented in Multisim. Multisim offers additional features such as ease of implementation, rebuild and cost reduction when compared to practical simulation of Flash ADC.**

Keywords— **Flash ADC, Comparator, Encoder, Hex, Resolution, 3and 8Bit, Multisim.**

I. INTRODUCTION

With the rapid growth of modern communications and signal processing systems, handheld wireless computers and consumer electronics are becoming increasingly popular. Mixed-signal integrated circuits have a tendency in the design of system-on-chip (SOC) in recent years. SOC designs have made possible substantial cost and form factor reductions, in part since they integrate crucial analog interface circuits, such as ADCs with digital computing and signal processing circuits on the same die [1]. At present scenario, analog to digital converters find applications in communications, high-definition television set top boxes, video projectors, MP3 players and video equipment such as Digital Video Disk (DVD) players, High definition Digital Television (HDTV) and numerous other products. ADCs are interfaced with digital circuits in mixed signal integrated chips, where digital signal processing is performed. The supply voltage for digital devices is decreasing rapidly as the technology scales. Analog to digital converters are required to be operating with these devices, preferably at the same voltages. If the analog and digital components on a chip are not operating at the same supply voltage, then level converters need to be incorporated. In the symbol and block diagram form, it can be represented as such (Figure1and 2) :.

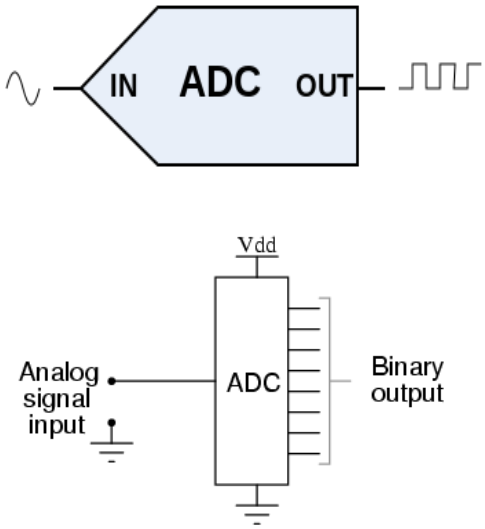

Fig 2: Basic block diagram of an analog-to-digital converter

II. FLASH ADC

A flash ADC is called "flash" because of its speed in performing conversions. Flash analog-to-digital converters, also known as parallel ADCs, its fastest way to convert an analog signal to a digital signal and basic 3 bit flash ADC circuit is shown Figure 3. Flash ADCs are suitable for applications requiring very large bandwidths. However, these converters consume considerable power, have relatively low resolution, and can be quite expensive. This limits them to high-frequency applications that typically cannot be addressed any other way. Typical examples include data acquisition, satellite communication, radar processing, sampling oscilloscopes, and high-density disk.[2]

The flash converter is the highest speed ADC available, but is required much more circuitry then other types. For example 3bit Flash ADC required 7 analog comparators, 6bit Flash ADC requires 63 analog comparators, while an 8bit unit requires 255 comparators and a 10bit converter requires 1023 comparators. The large number of comparators has limited the size of Flash convertors.

II a. Three Bit Flash ADC

Illustrated is a 3-bit flash ADC with resolution 1 volt (Figure 3). The resistor net and comparators provide an

input to the combinational logic circuit, so the conversion time is just the propagation delay through the network - it is not limited by the clock rate or some convergence sequence. It is the fastest type of ADC available, but requires a comparator for each value of output (63 for 6-bit, 255 for 8-bit, etc.) Such ADCs are available in IC form up to 8-bit and 10-bit flash ADCs (1023 comparators) are planned. The encoder logic executes a truth table to convert the ladder of inputs to the binary number output.

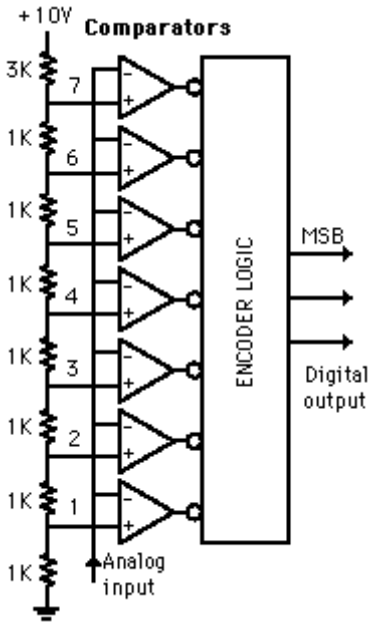

Fig 3: Three BIT ADC Block diagram

The Flash ADC is the fastest and also the simplest of the ADC schemes 2, 3,5 and 8. It is designed using a voltage divider connected to a series of comparators and an encoder. Figure 4 shows how the comparators in a flash converter are organized. It uses a reference voltage at the full-scale (FS) of the input range and a voltage divider. The latter is composed of 2n + 1 resistors in series, where n is the ADC resolution in bits. The value of the input voltage is determined by using a comparator at each of the 2n reference voltages created in the voltage divider. Flash converters are very fast (up to 500 MHz or more) because the bits are determined in parallel. This method requires a large number of comparators, thereby limiting the resolution of most parallel converters to 8 bits (255 comparators).

II b. Comparator

The comparator circuit work by simply taking two analog inputs, comparing them and produce the logical output high "**1**" or low "**0**".By applying the analog signal to the comparator + **input** called "**non-inverting**" and - **input** called "**inverting**", the comparator circuit will compared this two analog signal, if the analog input on + **input** is greater than the analog input on - **input** (inverting) then the output will swing to the logical "**1**" [3]

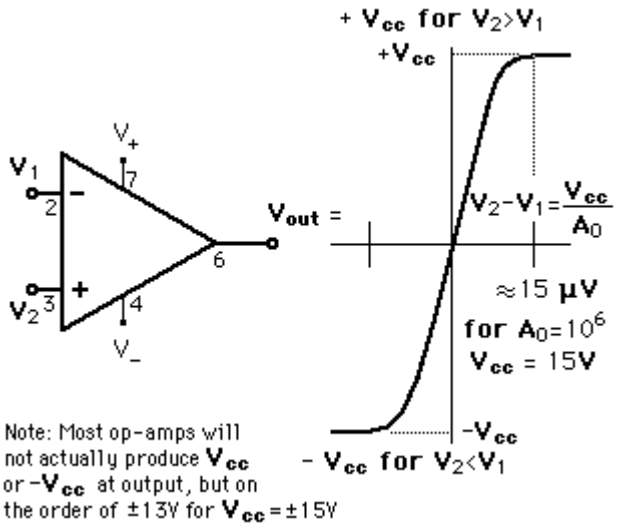

Fig 4: Comparator design

The extremely large open-loop gain of an op-amp makes it an extremely sensitive device for comparing its input with zero. For practical purposes, if the output is driven to the positive supply voltage and if V2 < V1 it is driven to the negative supply voltage. The switching time for - to + is limited by the slew rate of the op-amp.

III. MULTISIM , CIRCUIT, RESULTS

The Multisim simulator is software simulation tools which provide an accurate simulation of digital and analog circuit operations. Multisim allows us to grasp concepts quicker and gain deeper intuition for circuits. The operating system windows XP/ Vista / 64bit Vista and Windows supports fully to this Multisim software. It has been designed to help hardware designers' gain better understanding of circuit behavior. [4] Since the quality of simulation results is highly dependent on applied signals as well as analyzing and displaying simulation. It helps to close gap between design and practical test. It is easier to interface real world signal from inside Multisim and output data to drive real world circuitry, or display simulation data in a more suitable to form. Using this software it's possible to design projects before it is executed on real components. Multisim provides with an interactive oscilloscope, bode plotter, logic analyzer, and power supply, multimeter, function generator, etc. to simulate and analyze the design. It trains creative thinking and innovative abilities. Therefore, the use of Multisim is able to meet the needs of the electronic experiment curriculum design.

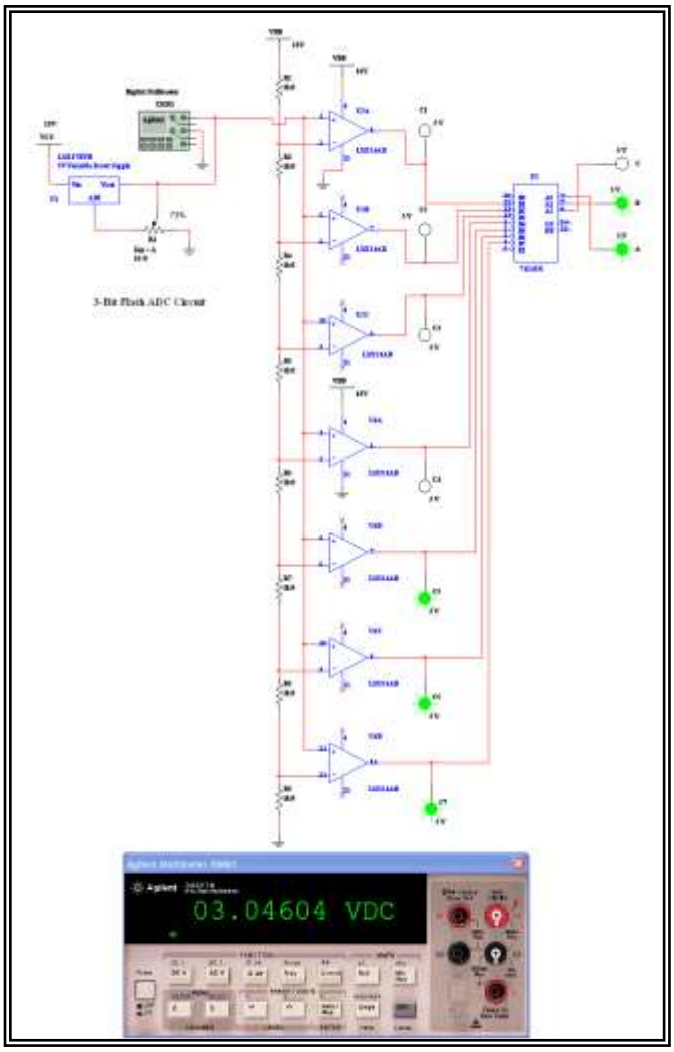

Fig 5 : Schematic diagram of 3bit Flash ADC and output

III a. Computer Simulation

Referring to Fig 5 we see an adjustable reference voltage power supply using 117 (regulator) available to +Vref via voltage supply Vout and potentiometer R1. The varying analog input signal is also derived from Vout using potentiometer R1 to provide signal variation to the VIN input of the ADC.

Additionally, we note –Vref (VREFN) pulled to ground to enable the unipolar output operation. The SOC (Start of Conversion) pin is tied to a square wave signal generator to provide the necessary clock source to ensure continual updating of the ADC.

After defining voltage divider and the other components simulate the ADC circuit using Multisim, which is a software for circuit design, with digital voltmeter. [5] Fig 5. shows the Multisim simulation Analog input (03.04604VDC) and Digital output (LED 011)

III b. Result

TABLE 1 Bit Flash ADC circuit Experimental readings.
(Comparator and Digital o/p)

3-Bit Flash ADC outputs										
Analog Input	**Comparator o/p**							**Digital o/p**		
V_A	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C	B	A
0.00000V to 0.943664V	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*
1.14343V to 1.97404V	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*	*0*	*1*
2.17705V to 2.82995V	*0*	*0*	*0*	*0*	*0*	*1*	*1*	*0*	*1*	*0*
3.04604V to 3.87269V	*0*	*0*	*0*	*0*	*1*	*1*	*1*	*0*	*1*	*1*
4.07910V to 4.89207V	*0*	*0*	*0*	*1*	*1*	*1*	*1*	*1*	*0*	*0*
5.08268V to 5.88465V	*0*	*0*	*1*	*1*	*1*	*1*	*1*	*1*	*0*	*1*
6.08365V to6.88113V	*0*	*1*	*1*	*1*	*1*	*1*	*1*	*1*	*1*	*0*
7.05592V to 10.000V	*1*	*1*	*1*	*1*	*1*	*1*	*1*	*1*	*1*	*1*

The Flash ADC convertor in Figure 5 has a 3bit resolution and step size of 1V. The voltage divider sets up reference levels for each comparator so that there are seven levels corresponding to 1V, 2V, 3V,……. and 7V(Full scale). The analog input. V_A is connected to the other input of each comparator. Analog input and comparator output and finally Digital output shown in Table 1.
When operated, the flash ADC produces an output that looks something like this:

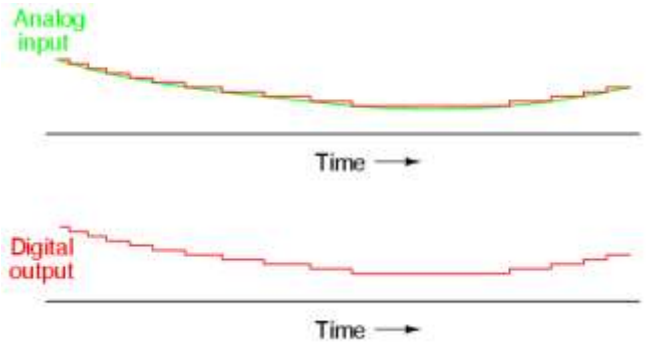

Fig 6 : Analog input and Digital output

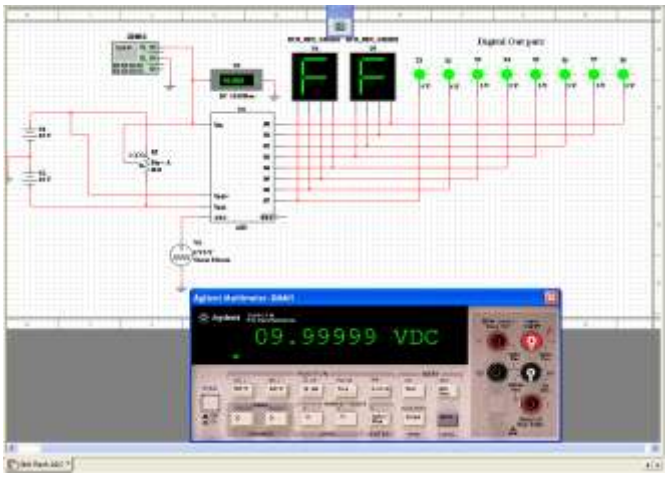

Fig 7: Schematic Diagram of 8bit Flash ADC and output.

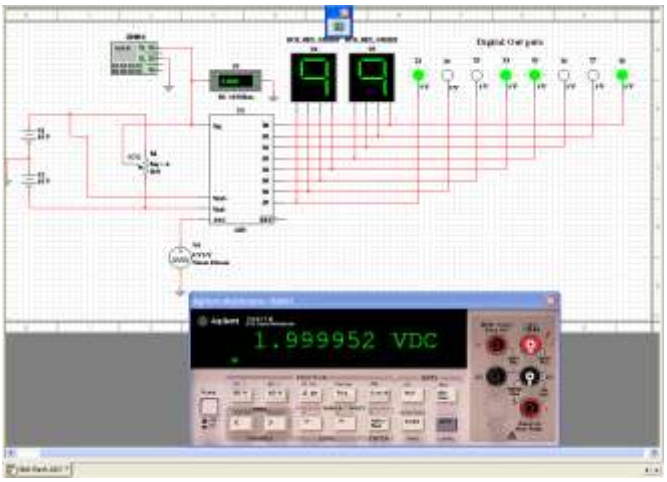

Fig 8: Schematic Diagram and output of 8bit Flash ADC.

The circuit of A-to-D converter shown here is configured around ADC, avoiding the use of a microprocessor. The ADC is an 8-bit A-to-D converter, having data lines X1 to X8. It works on the principle of successive approximation. In analog input channel Vin as usually the control signals EOC (end of conversion), SOC (start of conversion), Vref + and Vref - are interfaced by means of a microprocessor. However, the circuits shown (Fig 7 and 8) here is built to operate in its continuous mode without using any microprocessor. Therefore the input control signals Vref + and Vref - being active-high, are tied to Vcc (+10volts to -10volts). The input control signal SOC, being active-low, initiates start of conversion at falling edge of the pulse, whereas the output signal EOC becomes high after completion of digitisation. This EOC output is coupled to SOC input, where falling edge of EOC output acts as SOC input to direct the ADC to start the conversion. As the conversion starts, EOC signal goes high. At next clock pulse EOC output again goes low, and hence SC is enabled to start the next conversion. Thus, it provides continuous 8-bit digital output corresponding to instantaneous value of analogue input. The maximum level of analogue input voltage should be appropriately scaled down +10volts to -10volts level, same continues as shown in Table 2.

Table 2: 8 Bit Flash ADC Simulated output with Hex values (Digital o/p)

8 – Bit Flash ADC output									
Decimal Equivalent	Analog Input mV / V	Hex Value	Digital outputs							
			X1	X2	X3	X4	X5	X6	X7	X8
0	-9.99999	00	0	0	0	0	0	0	0	0
12	-8.99995	C	0	0	0	0	0	1	1	0
51	-5.99990	33	0	0	1	1	0	0	1	1
64	-4.99991	4C	0	1	0	0	0	0	1	1
128	0.00000	80	0	1	0	0	0	0	1	1
153	**1.99995**	**99**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**
191	4.99930	BF	1	0	1	1	1	1	1	1
204	5.99990	CC	1	1	0	0	1	1	0	0
230	7.99992	E6	1	1	1	0	0	1	1	0
255	**9.99999**	**FF**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

In Table 2 only few cases have been shown and rest have been ignored due to larger decimal equivalent (ie 0 -255)

IV. Design 3 bit Flash ADC

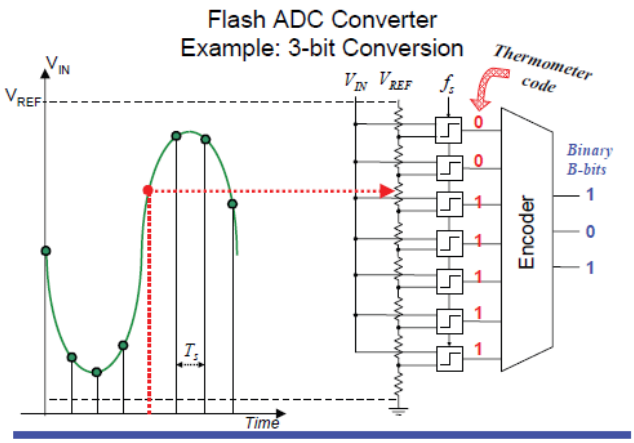

Fig 9: A block diagram of the proposed Flash ADC design

The flash type ADC consists of an array of parallel comparators that is fed a threshold voltage derived from a reference voltage and potential divider to the inverting input terminal of the op-amp comparator and the input analog voltage to the non-inverting input terminal of the op-amp. On crossing the threshold (the voltage at the inverting input), the output of the comparator goes high[6]. Since the threshold is derived from a potential divider, each comparator is set to go high at different threshold levels. However, as comparator for level n goes high, all comparator below n go high as well. So, a priority encoder is used to convert these input lines form the comparator into binary coded output. The priority encoder accepts an 8 line input and gives out a 3 bit binary output. (Figure 9)

IV a. Resolution and Examples

The resolution of the converter indicates the number of discrete values it can produce over the range of analog values. The values are usually stored electronically in binary form, so the resolution is usually expressed in bits. In consequence, the number of discrete values available, or "levels", is usually a power of two. For example, an ADC with a resolution of 8 bits can encode an analog input to one in 256 different levels, since $2^8 = 256$. The values can represent the ranges from 0 to 255 (i.e. unsigned integer) or from −128 to 127 (i.e. signed integer), depending on the application. Resolution can also be defined electrically, and expressed in volts. The minimum change in voltage required to guarantee a change in the output code level is called the LSB (least significant bit, since this is the voltage represented by a change in the LSB). The resolution Q of the ADC is equal to the LSB voltage. The voltage resolution of an ADC is equal to its overall voltage measurement range divided by the number of discrete voltage intervals:

$$Q = \frac{E_{\text{FSR}}}{N},$$

Where N is the number of voltage intervals and EFSR is the full scale voltage range. E_{FSR} is given by

$$E_{\text{FSR}} = V_{\text{RefHi}} - V_{\text{RefLow}},$$

Where V_{RefHi} and V_{RefLow} are the upper and lower extremes, respectively, of the voltages that can be coded.

Normally, the number of voltage intervals is given by

$$N = 2^M,$$

where M is the ADC's resolution in bits.

IV b. Some examples:

Example 1

Full scale measurement range = 0 to 10 volts

ADC resolution is 12 bits: 212 = 4096 quantization levels (codes)

ADC voltage resolution, Q = (10 V − 0 V) / 4096 = 10 V / 4096 ≈ 0.00244 V ≈ 2.44 mV.

Example 2

Full scale measurement range = -10 to +10 volts

ADC resolution is 14 bits: 2^{14} = 16384 quantization levels (codes)

ADC voltage resolution is, Q = (10 V − (−10 V)) / 16384 = 20 V / 16384 ≈ 0.00122 V ≈ 1.22 mV.

Example 3

Full scale measurement range = 0 to 7 volts

ADC resolution is 3 bits: 2^3 = 8 quantization levels (codes)

ADC voltage resolution is, Q = (7 V − 0 V)/7 = 7 V/7 = 1 V = 1000 mV

Binary Number System for one byte									
Bit Number	8	7	6	5	4	3	2	1	0
Bit Weight	256	128	64	32	16	8	4	2	1

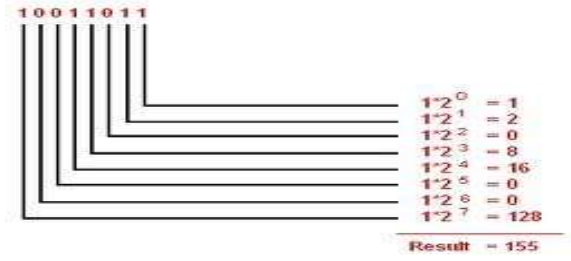

Fig 10. Design Example 8 – bit Flash ADC (case 155)

III a. Defining the Components

1. Digital Voltmeter: A digital voltmeter is an instrument that measures the voltage of any low power circuit, and displays the value on a digital display.

2. Voltage Divider : In order to design voltage divider in 3bit ADC needed a total of Severn 1 kW resistors. Since I=V/R, with an 10V input and 7 kW total, the current = 1mA. Therefore, each resistor drops 1V. The non inverting inputs of comparators one through ten are at 1V to 10V successively.

3.LM324AD : The LM324AD chip contains four comparators. For our design, we utilized Two chips, which in total gave us the Seven comparators we needed plus one, which were not utilized [7].

4.74148N : It's a 8-to-3 Priority Encoder. The 74148 encoder converts the output of the comparators to a true binary coded decimal (BCD) form.

5. ADC : 3 bit and 8bit Analog to Digital converter.

6. Seven Segment Display: The seven-segment display actively shows its state while the circuit is running. The seven terminals (left to right, respectively) control segments A to G. By giving the proper binary-digit inputs to segments a to g, you can display decimal numbers from 0 to 9 and letters A to F.

V. CONCLUSION

For applications requiring modest resolutions, typically up to 8-bits, at sampling frequencies in the high hundreds of MHz, the flash architecture may be the only viable alternative. The user must supply a low-jitter clock to ensure good ADC performance. For applications with high analog-input frequencies, the ADC chosen should have an internal track-and-hold. The concept of a Flash ADC has been successfully developed, implemented and simulated. Future work on this will be to continue to perform other tests and to expand the read-out to have more than 8bit reading. The Multisim simulator is a useful tool to perform theoretical and practical experiments to improve understanding of the various electronic concepts. It is also helpful to design and program embedded system applications in our further research work. It also can debug, execute verify results before real time implementation. Experiments were performed on 3 bit and 4 bit Flash ADC with comparator and Seven segment display (Hex values) Results shows higher range of accuracy is obtained when Flash ADC is experimented in Multisim, It also offers additional features such as ease of implementation, rebuild and cost reduction when compared to practical simulation of Flash ADC.

VI. REFERENCE

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Raghavendra.R Diploma in electronics and Communication in the year 2000, and currently working in RV College of Engineering, Mysore road, Bangalore, Karnataka, India as a Instructor. His main research interests include electronic circuits design and debugging, Microcontroller, Genral perpose PCB designing, Networking, servicing, soldering and desoldering.

Dr Hariprasad S.A obtained his PhD from Avinashilingam University for Women, Coimbatore in the area of digital controllers .He is having teaching experience of 23 years and six years of research experience. He has published 35 papers in international national journals and conferences. He has also published a text book on advanced Microprocessor and reviewed books on Microwave engineering and won best teacher award (twice) from RSST and appreciation award from ISTE. His research areas of interest are embedded systems and RF systems.