Area Efficient FPGA Based Bidirectional Network on Chip Router through Virtual Channel Regulator

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***Abstract*—Fundamental unit of building a Network on Chip is the router; it directs the packets according to a routing algorithm to the desired host. Both NoC performance and energy budget depend heavily on the routers' buffer resources. This paper introduces a novel Bidirectional Network on chip router with unified buffer structure, called the dynamic Virtual Channel Regulator, which dynamically allocates Virtual Channels (VC) and buffer resources according to network traffic conditions. In this study, we analyse the move towards Networks-on-Chips router from an area and power perspective by accurately modeling a Bidirectional Network-on-chip router through Virtual Channel Regulator in FPGA. Accurate speed, area and power metrics are also reported for the networks router, which will allow a more complete comparison to be made across the NoC architectural router space considered. The proposed architecture of BiNoC router is simulated in Xilinx ISE 9.1i software. We designed a router with scalability feature which is synthesized in models of Virtex-II XC2VP30 FPGA infrastructures. The source code is written in VHDL. In addition, the proposed router uses low resource utilization percentage of FPGA. From the implementation results, the proposed router is operated with higher speed, area in terms of slices reduced by 11.14% and the LUTs reduced by 37.68%**

***Keywords*—Interconnection networks, on-chip communication, Reconfigurable, NoC, FPGA**

I. INTRODUCTION

The main purpose SoC system is to shrink the size of the chip as smaller as possible while seeking at the same time for more scalability, lower latency and higher bandwidth [1], [2].Conventional bus-based-systems are no longer reliable architecture for SoC due to a lack of scalability and parallelism integration, high latency and power dissipation, and low throughput. In the forthcoming era scalable global on-chip communications represent the only solution for many-core computing networks- on-chips (NoCs) [1].Networks-on-Chip (NoC) [1], [3] architectures are becoming the network fabric for both general-purpose chip multi-processors and application-specific systems-on-chip designs. In the design of NoCs, lower area and lower power overhead are both important design parameters and the router micro architecture plays a vital role in achieving these performance goals. NoC connects CPU, DRAM, SRAM and DMA other custom designs together using switching packets instead of switching messages or words, allowing NoC to provide a higher performance and higher bandwidth. On the other hand, the need for a high performance system that handles increased complexity becomes really important.

A typical NoC consists of computational processing elements (PEs), network interfaces (NIs), and routers shown in fig.1. The NI is used to packetize data before using the router backbone to traverse the NoC. Each PE is attached to an NI which connects the PE to a local router. When a packet was sent from a source PE to a destination PE, the packet is forwarded hop by hop on the network via the decision made by each router. For each router, the packet is first received and stored at an input buffer. Then the control logics in the router are responsible to make routing decision and channel arbitration. Finally, the granted packet will traverse through a crossbar to the next router, and the process repeats until the packet arrives at its destination. The NoC architecture consists of data link, network and transport layer. The wiring is done using the physical layer.

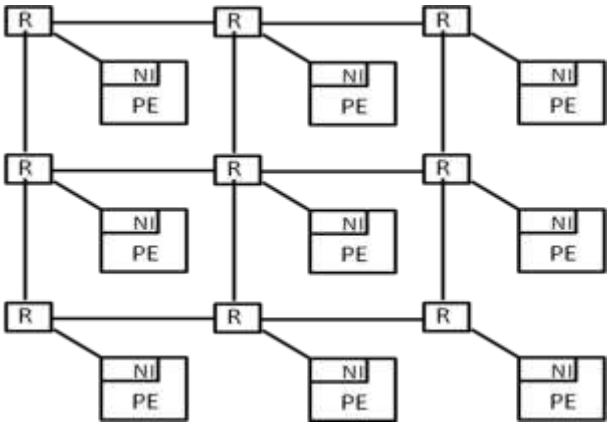

Figure 1. Typical NoC architecture in mesh topology

Bidirectional communication in the NoC typically employs fullduplex communication using two simplex links [4], [5]. We observed that there may be several scenarios as mention below where we may require bidirectional configuration control to get improve channel bandwidth capacity.

a. Assuming all the transactions of flits are flowing in a single direction, there might be situations in inter task connections where a certain link requires an increase in link capacity

b. Bandwidth requirements of transmission increases according to user requirement changes (e.g. the MPEG

processing element (P.E.) wants to switch video resolution to a higher resolution). If in such a scenario current channel capacity of one half of the duplex channel cannot meet the requirement then the other half can be reversed to add more available bandwidth (doubled the channel capacity in our bidirectional router)

c. When a faulty situation occurs in a simplex channel, the transmission of flits via this channel will not possible. In such a scenario, if another simplex channel has the ability to reverse its direction while free, it could transmit flits. Therefore, it increases the resource utilization and improves reliability factors through channel control module.

To the best of our knowledge, there has been very little work done for modification of generic virtual channel for BiNoC router. In this work, we are reviewing on virtual channel regulator module for BiNoC architectures. In BiNoC router unified buffer structure, called the dynamic Virtual Channel Regulator, which dynamically allocates Virtual Channels (VC) and buffer resources according to network traffic conditions.

The rest of this paper is organized as follows. In Section II, we will discuss some of the background materials for on chip router buffers. In section III, Motivation. Next section IV, Baseline of bidirectional network on-chip (BiNoC) architecture. In section V, over view of NoC router and section VI, shows bidirectional CDC. Finally, in Section VII, experiment results shows final router RTL and test bench waveform of Inter-router data transmission scheme along with Area comparison of proposed router with existent router. In last section, brief statements conclude this paper.

II. Related work

Flit-Bless proposed a routing scheme to send all incoming packets to output ports; irrespective of the fact whether those output ports are productive [6]. Buffer less routing is another novel and unique approach which eliminates all input buffers without utilizing channel buffering.

Z. Lu et. al. [7] proposed wormhole routing method in order to remove the blocking problem introduced if the head of packet is blocked during data transmission, the router cannot transfer the packet any more.

J. Hu et. al. [8] introduced the Buffer allocation and flit control to perform at a flit level in wormhole routing since wormhole routing does not allocate available buffer to whole packet. In a single transmission transferred, the wormhole router splits the packet into several flits.

H. Wang et. al. [9] introduced reduce or eliminate the size of input buffers. Recently iDEAL router proposed to reduce the size of the input buffers and utilize repeaters. This design reduces the number of input buffer to half but with the cost of increased complexity and latency. Other designs targeting power saving with router design have different approaches.

C. A. Nicopoulos [10] proposed Virtual Channel Regulator for dynamic buffering resources allocation focuses on efficiently allocating buffers to all virtual channels, by deploying a unified buffering unit instead of a series of separated buffers, and minimizing the required size.

In addition, VCs are used to avoid deadlock problem and thus increase throughput. The main purpose of VCs is to decouple the allocation of buffer space to allow a flit to use a single physical channel and competing with other flits. There are existing two router techniques based on wormhole and other based on virtual channel.

III. Motivation

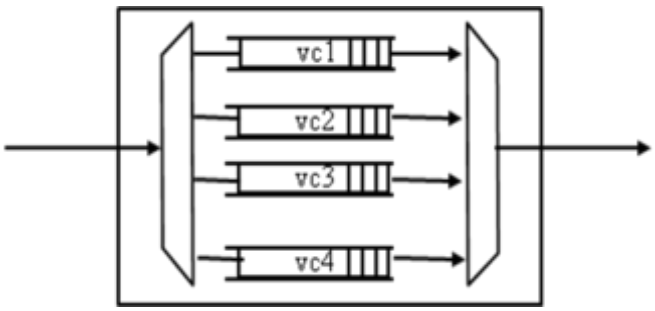

Figure 2. Generic Virtual Channel

A statistically allocated buffer used by a generic router which can cause the Head-of-Line blocking problem. In order to improve the network performance [8] Proposes buffer customization which decreases the queue blocking probability as shown in fig.2.The dynamic buffer allocation significantly increases buffer usage. A scheme called dynamic virtual channel regulator is proposed in [10]. In the virtual channel regulator, VCs are allocated dynamically, and buffer allocation for each VC could be different depending on network traffic.

IV. Generic Bidirectional Router Architecture

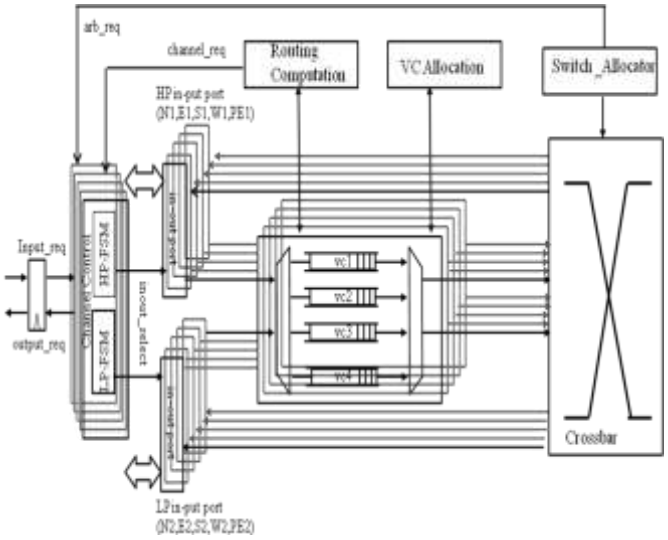

Figure 3. Generic Virtual channel router architecture for our BiNoC router .

At the heart of the data network are the routers. Depending on topology and on the number of IPs attached to them the routers have a variable number of input and output ports. In a packet switched network, the functionality of the router is to forward

an incoming packet to the destination resource if it is directly connected to it, or to forward the packet to another router connected to it. In the NoC architecture there are two routers the conventional router and the bidirectional router. In this conventional router the data can be send in only one direction whereas in bidirectional router the data can be send and receive simultaneously. The Bidirectional Network on Chip (Bi-NoC) architecture is more efficient than the conventional architecture because in conventional architecture the unidirectional flow is used where as in Bi-NoC the two way data flow can be performed [11] shown in fig 3.

V. OVERVIEW NETWORK-ON-CHIP ROUTER

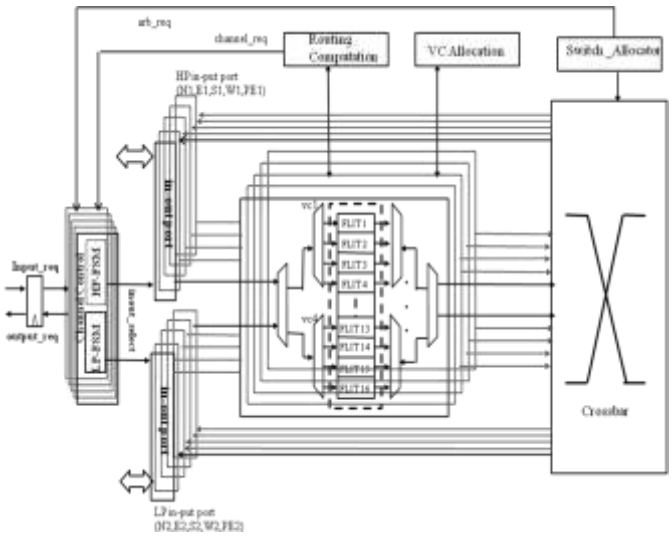

Figure 4. Modified Virtual channel router architecture for our BiNoC router with four state pipelines.

Fig.4 illustrates the major components of a Bidirectional Network-on-Chip Router through Virtual Channel Regulator. The basic steps undertaken by a router are enumerated below:

A. Virtual Channel Regulator

Buffer architecture for virtual channel regulator is shown in Fig.5.The router implemented using virtual channel through Virtual Channel Regulator [10].This can efficiently allocating buffers to all virtual channels, instead of using separated buffers, a unified buffer structure (UBS) is used to share the internal flit buffers and Control Logic to control UBS and assign buffers into VCs dynamically according to the network traffic. It is shown in the Fig.5 that UBS is similar to generic buffer structure in which the v independently k-flit are logically grouped in a single vk-flit and with CL as logically unified structure. To avoid large components UBS has the same number of MUX/DEMUX i.e. one MUX/DEMUX per k flits. In this logic, the first stage reduces the number of requests from each input VC to one and the winning request from each input VC proceeds to the second arbitration stage. The CDC routing algorithm is used to perform the architecture. The Bi-NoC architecture allows each channel to transmit in all direction and increases the bandwidth, reduces the access latency, and reduces power consumption.

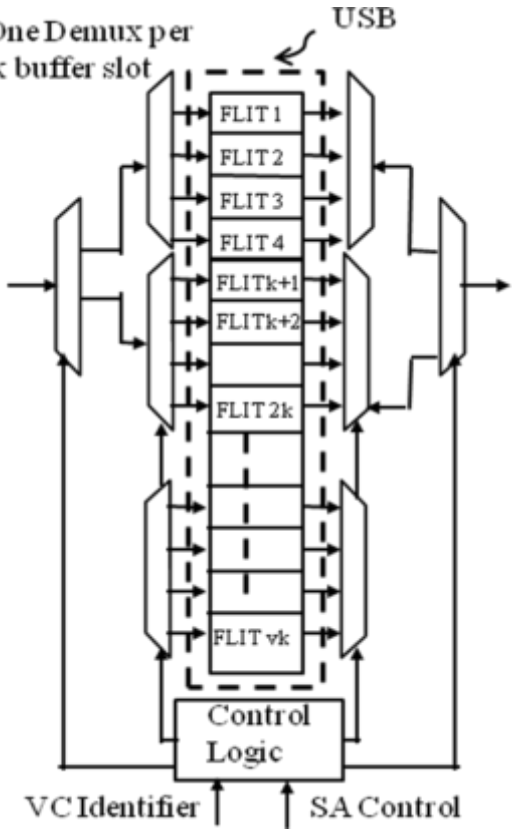

Figure 5. Virtual Channel Regulator

B. Router Pipeline

A generic on-chip router consists of multiple atomic pipeline stages shown in fig.5; Routing Computation (RC), Virtual Channel Allocation (VA), Switch Allocation (SA), and Switch Traversal (ST) router pipelines as shown in Fig.6. Many researchers have proposed router architectures that reduce the router pipelines along the critical path by parallelizing some of these stages, thereby achieving low latency routers [12-14].The BiNoC architecture assumed in this paper is a four stage pipelined router which allows the RC, VA, and SA stages to execute in parallel.

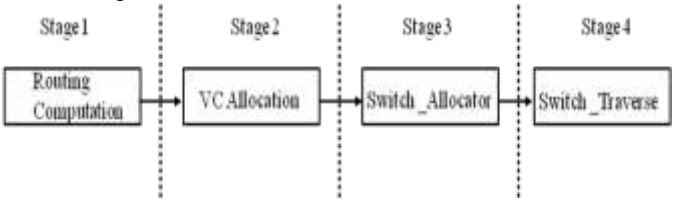

Figure 6. Typical four stage pipelined router design based on VC flow control.

C. Reconfigurable Input/Output Ports

The ports in the bidirectional are reconfigurable. This is done by using the local information.

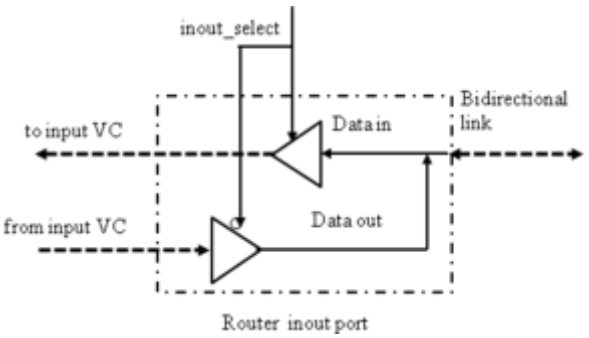

Figure 7. Schematic of Reconfigurable Input/Output Ports implemented in BiNoC architecture.

As shown in Fig.7, the input and output port used in bidirectional NoC architecture is based on the priority. In this one port is designed with the higher priority and the other port is designed with the lower priority. A channel control protocol is used to determine its own transmission direction from a router to another router. By this bidirectional ports doubling of channel bandwidth is possible.

VI. Channel Direction Control Module

The flow direction at each channel is controlled by a channel direction control (CDC) algorithm. Two major functions performed by the channel control algorithm.

1. Dynamically configure the channel direction between neighboring routers.

The control algorithm is implemented with two finite state machines. The current status of channel direction decides whether the channel request for corresponding channel is blocked or not.

2. To process the channel allocation by sending arbiter request to the switch allocator.

The channel direction control algorithm replaces all the unidirectional channels in a typical NoC with bidirectional channels. The HP and LP ports of each router use two FSMs, a HP FSM and a LP FSM are connected to bidirectional channel. Pair of signals input−req and output−req is used to exchange information between two FSMs.

A. Bidirectional Channel Direction Control

The finite state machine diagrams for a High priority and a Low Priority Channel Direction Control algorithm are shown in Fig.8 (a) and (b), respectively. Each FSM has three states: free, wait, and idle.

a. Free State: the channel is ready for data to send (output) the adjacent router.
b. Idle state: the channel is available to receive (input) data from the adjacent router.
c. Wait state: it is an intermediate state ready to transition from idle state with input channel to free state with output channel.

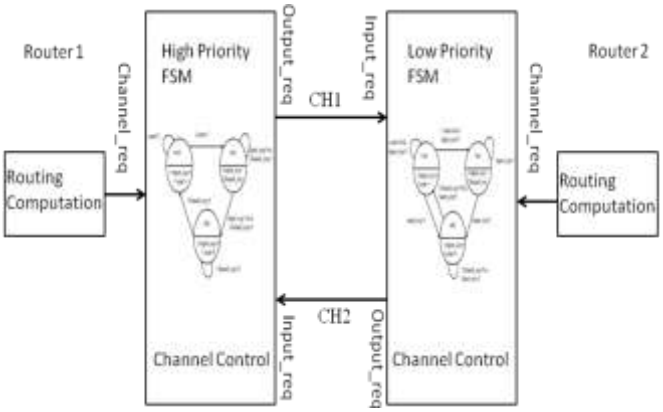

Figure 8. (a) FSM for HP port and (b) FSM for LP port for bidirectional channels between two neighbouring routers .

VII. Experimental Results Performance Evaluation

In this section, we present simulation-based performance evaluation of our architecture, BiNoC router with VC flow-control technique in terms of network Area, energy consumption. In this we are using the Spartan XC3S50 FPGA to functionally verify the stand alone router. We use the Xilinx 13.1i to synthesis. The BiNoC architecture increases the speed in the router. Since the virtual channel regulator is used it avoids the deadlock condition and the packets transferred need not to be waited for long time to reach the destination. The size of the architecture is minimized and hence the power consumption is reduced in bidirectional NoC architecture. This architecture performs self-reconfigurable; it is done using the local information. The access latency is very less while using this architecture. Unfortunately, at present, there are no readily accessible FPGA based router architecture systems with which we can make meaningful comparisons. We describe our experimental methodology, and detail the procedure followed in the evaluation of these architectures.

A. Simulation Setup

In this section, the synthesis results will be presented. We evaluate the reconfigurable virtual channel regulator BiNoC in terms of power dissipation, area overhead and overall network performance. We consider 4-stage pipelined router design. Each router has P = 10 inout ports (8 for inout direction and 2 for the inout PE. The baseline design considered has 4 VCs (UBS) per input port, with each VC having 4 flit buffers in the router, for a total of 160 flit buffers (= 10× 4 × 4). Each packet consists of 16 flits and each flit is 128 bits long. In each case, the design is implemented in VHDL language on RTL level and synthesized using the Xilinx ISE 13.1i tool. The proposed router was prototyped in Spartan XC3S50 FPGA technologies. Table I presents our router results with the same flit size and FPGAs used by Generic Router.

B. Bidirectional NoC Router Validation

The Bidirectional NoC Router through virtual channel regulator was described in VHDL and validated by functional simulation. Fig.8 shows functional simulation result of Inter-router data transmission scheme in BiNoC router. This simulation is performed on Active-HDL software.

a. *Final Router RTL*

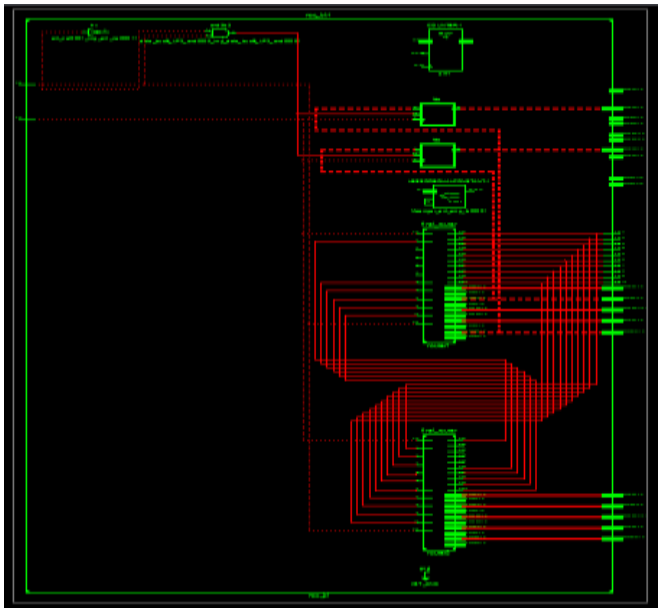

Figure 9. Inter-router data transmission scheme used for two bidirectional channels between a pair of routers.

b. Inter-router Test Bench Waveform

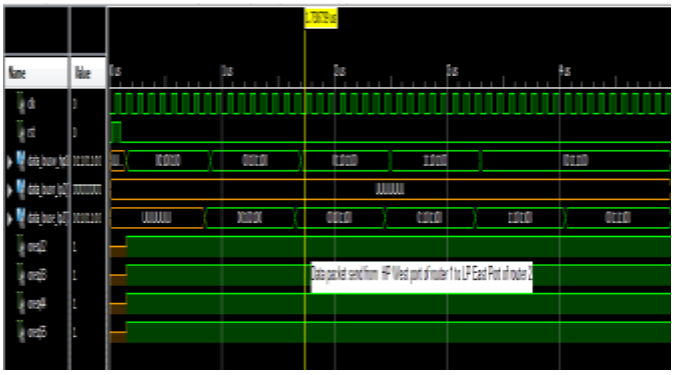

Figure 10. Test bench waveform for Inter-router scheme.

Fig.10 shows test bench waveform of Inter-router data transmission scheme used for two bidirectional channels between a pair of routers. A data packet of 16 flit send it from HP west port of router 1 to LP East Port of router 2.fig.9 shows final router RTL for Inter-router data transmission scheme.

C. Area breakdown and performance analysis

Unfortunately, few authors have published implementation results directly for their proposed FPGA NoC architectures router. As a result, it is difficult to perform direct comparison with other network approaches.The router area, power and speed were estimated for comparison with other works. The operating frequency is 165.455MHz and data arrival time is 4.30 ns. Table I presents our router results with the same flit size and FPGAs used by authors of other works.

TABLE I. OUR ROUTER RESULTS WITH THE SAME FLIT SIZE AND FPGAS USED BY GENERIC ROUTER.

Resources	5 Port Router				
	avail	Generic Router	Utility %	Proposed Router	Utility %
slices	768	696	90%	510	66%
Flip-Flops	1536	958	62%	523	34%
LUTS	1536	1004	65%	918	59%
IOBs	63	98	156%	102	161%

D. Area comparison with other router

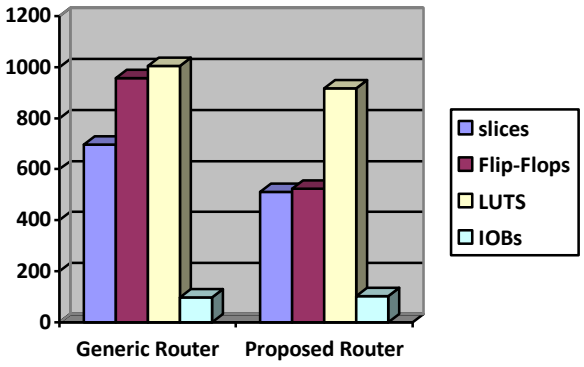

Figure 11. Area comparison of various FPGA Router.

The fig.11 shows that the Area in the proposed model is less than that of the existing system. There is an efficient reduction in the number of slices, slice flip flops and input LUTs in the proposed system than those obtained in the existing generic router these reduction rates are given as, The slices reduced by 26.72%, the number of flip flops reduced by 45.40% and the input LUTs are reduced by 8.56%.

E. Power breakdown

The total power consume for a 128-bit flit in the buffer is estimated to be 27mW in Spartan XC3S50.

F. CONCLUSION

This paper proposed methods to increase the overall performance of NoC routers. A flexible network design gives

the opportunity to easily search the design space for an optimum solution as well as to quickly develop the communication infrastructure of a new system. Networks on chip can have different requirements in terms of area and power depending on the application domain they are targeted at. This work presented the implementation of BiNoC router through virtual channel regulator concept. The synthesis and simulation of the proposed router is verified through VHDL codes using XILINX ISE 13.1i software. When compared to previous publications about FPGA based NoCs router, our implementation has either smaller area, higher clock frequency. There is an efficient reduction in the number of slices, flip flops and input LUTs in the proposed system than those obtained in the existing. These reduction rates are given as, the slices reduced by 26.72%, the number of flip flops reduced by 45.40% and the input LUTs are reduced by 8.56%.

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